Multidisciplinary Applied Research and Innovation Vol. 2 No. 3 (2021) 130-134

MARI

Homepage: http://publisher.uthm.edu.my/periodicals/index.php/mari
e-ISSN :2773-4773

Automated Home Controller Design with ASIC Implementation

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DOI: https://doi.org/10.30880/mari.2021.02.03.026
Received 05 September 2021; Accepted 05 October 2021; Available online 15 December 2021

Abstract : Safety and quality of the living environment for tenants can be incorporated by home automation technologies which could monitor and control the household applications. The current penetration of the home automation system in the market is low due to its system complexity, power consumption, lack of security system, and service interruptions upon power outages. Thus, this design aims to develop a compact and low power automated home controller that integrated comfort control, security system and automated load transfer switch feature, which advanced from the previous studies in terms of security and backup power for the home automation system. The pulse width modulation (PWM) technique is implemented in the lighting system control to enhance the energy efficiency of the home automation system. The design is developed with Verilog Hardware Descriptive Language (HDL), while a testbench for each module is written for functional verification via Synopsys VCS. To develop an integrated automated home controller with low power consumption and at the same time minimized the area, the design is optimized using 90nm TSMC process technology using Synopsys Design Compiler (DC) and Synopsys IC Compiler (IC) at logical synthesis and physical synthesis stages, respectively. In this project findings, 200Hz of duty cycle pulses is successfully simulated via PWM technique to allow the human eye not to discern light blinking during light dimming occasions in the lighting system in the top-level module. The final layout's total power consumption and area are successfully implemented with 65.61µW and 662.44μm^2, respectively. The proposed automated home system controller has successfully integrated the three features and functioned correctly by giving correct outputs while scaled down into a chip at Application Specific Integrated Circuit (ASIC) level with a small area and low total power consumption.

Keywords: Home Automation, Security, PWM, ASIC

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1. Introduction

The home automation system, also known as a "smart home," was incorporated with a single or more automated system in control of the operation of primary home devices spontaneously or remotely. The home automation system's three main system elements were divided into sensors, controllers, actuators [1]. The implementation of this system in Malaysia only contributed 10.7% in 2020 and is expected to increase 9.5% in 2025 [2]. Factors such as system complexity, lack of security system, and not incorporating emergency backup power and power consumption have hindered the system's popularity.

Based on the previous works, the simple home automation using Field-Programmable Gate Array (FPGA) proposed by S.Sharma et al. [3] developed the system using Verilog and implemented the FPGA as a control unit controlled several applications such as sliding door, air conditioner, and light only. In [4], the mechanized controller component was developed using FPGA to control the lighting and regulated the fan speed under room conditions only. Both systems are lack of security system. In [5], home automation and security integration into one complete system using FPGA had been proposed. However, it does not focus on home comfort control. The automation system proposed by S S.Vishwakarma and P. Jaiswal [6] aimed to provide security and comfort to the user, such as water overflow or fire alarm, mechanized lighting, and fan system using FPGA. The intelligent home model using Application Specific Integrated Circuit (ASIC) design flow had been presented in [7]. The system is fully developed using Verilog and enabled embedding various devices in terms of comfort and security. All the previous works presented do not consist of emergency backup power.

Hence, an advance automated home system controller had been proposed in this project. The proposed design is highly compact where it involved integrating three main systems: comfort control, security system, and automated load transfer switch using ASIC implementation. The design can prevent service interruption during power failure conditions by automating switching both primary and secondary power lines to the loads. Pulse Width Modulation (PWM) methodology is also implemented to control the ambient light for improving the lighting control's efficiency. Critical design parameters such as area, cell leakage, and dynamic power were considered in this project to realize a small and compact automated home system controller with low power consumption.

2. Materials and Methods

The top-level module, which integrates comfort control, security, and power outages prevention, was developed using bottom-up methodology via Verilog Hardware Descriptive Language (HDL). 100MHz clock frequency is set for the proposed design. A counter with a maximum value of 500000 used to design the PWM signal to generate a 200Hz pulses. Specifications for the Register Transfer Level (RTL) logic design for the three system is listed in Table 1.

Table 1: Design specification of the automated home system controller

Systems	Sub-Systems	Input Sensors	Conditions	Activated Outputs
Comfort Control	HAVC	LDR, IR Sensor, 8-bit Temperature Sensor	$16℃ \leq temp \leq 22℃$	Fan with Speed 1
			$22℃ < temp \leq 27℃$	Fan with Speed 2
			$27℃ < temp \leq 32℃$	Fan with Speed 3
			$temp > 32℃$	Aircon
			$temp < 16℃$	Heater
	Lighting		Nighttime & No Motion	40% Light Intensity
			Nighttime & Motion	100% Light Intensity

Security System	Window Alarm	Magnetic Switch Sensor & IR Sensor	Magnetic Switch Sensor =0 & Motion =1	Window Alarm & Red Light
Systems	Sub-Systems	Input Sensors	Conditions	Activated Outputs
	Fire Alarm	Smoke Sensor	Smoke Sensor =1	Fire Alarm & Red Light
Security System	Door Alarm	12-bit Hexadecimal Passcode Door Lock, Button	Passcode Input = Saved Password	Door Open & Green Light
			Button =1	Window Alarm & Door Alarm Deactivation
			Passcode Input ≠Saved Password	Trials Counter Count & Yellow Light
			Trials Counter =3	Door Alarm, Window Alarm, Red light and Yellow Light
Automated Load Transfer Switch	-	8-bit Solar Voltage & 8-bit Grid Voltage	$200V \leq Solar \leq 240V$	Solar Poweline
			$Solar < 200V$ & $Solar > 240V$	Grid Powerline
			$Grid < 200V$ & $Grid > 240V$	

After verifying the RTL logic design of each module using Synopsys VCS, the design is then loaded into the Synopsys Design Compiler for logical synthesis via 90nm TSMC technology library. Area and power of the design is optimized in high effort where the extra optimization is performed. Next, same technology library of 90nm TSMC used for the physical synthesis using Synopsys IC Compiler. The gate-level netlist is then loaded into the Synopsys IC Compiler. Then, a floorplan is created with 0.8 of core utilization ratio and the standard cells is placed next into the core area with power optimization followed by Clock Tree Synthesis (CTS). The signal nets routed next along with extra power optimization and replacing the existing cells with smaller cells during the post-route optimization. The final layout of the design is verified before signing off to GSDII file.

3. Results and Discussion

Figure 1 shows the functional verification for a 40% duty cycle using Synopsys VCS with a 1ns time unit. 200Hz pulses are successfully simulated same as the PWM technique proposed [8], to avoid the noticeable light flickering captured by the human eye during the light diming event. The simulated 40% duty cycle shown in the yellow box in Figure 2 is verified by its 2ms on time and 3ms off time, while the red box shows the 100% duty cycle with no off time. From Figure 2, all the actuators from the top-level module can respond according to the respective inputs given by the sensors based on the system's design specification in Table 1. This module enables the user to start security verification by confirming the input passcode and alarm disable the function with the button input along with the pre-fire alert system while checking and controlling other systems simultaneously. The pink color box in Figure 3 shows that the Solar was chosen as the default power line for reducing the electricity bills, and the controller will switch to grid power line once the voltage does not meet the specification If both power sources are unstable, grid power line will be chosen to prevent overuse of solar battery and wait for the solar recharged.

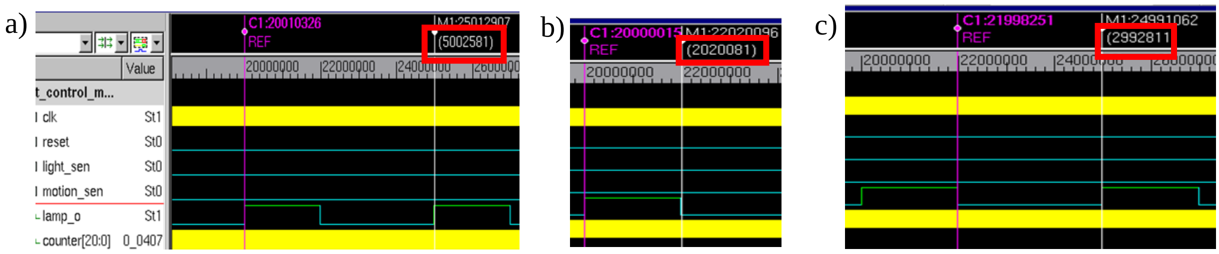

Figure 1: Output waveform of 40% duty cycle in lighting system with 10ns clock period a) 5ms of period pluses b) On time of 2ms c) Off time of 3ms

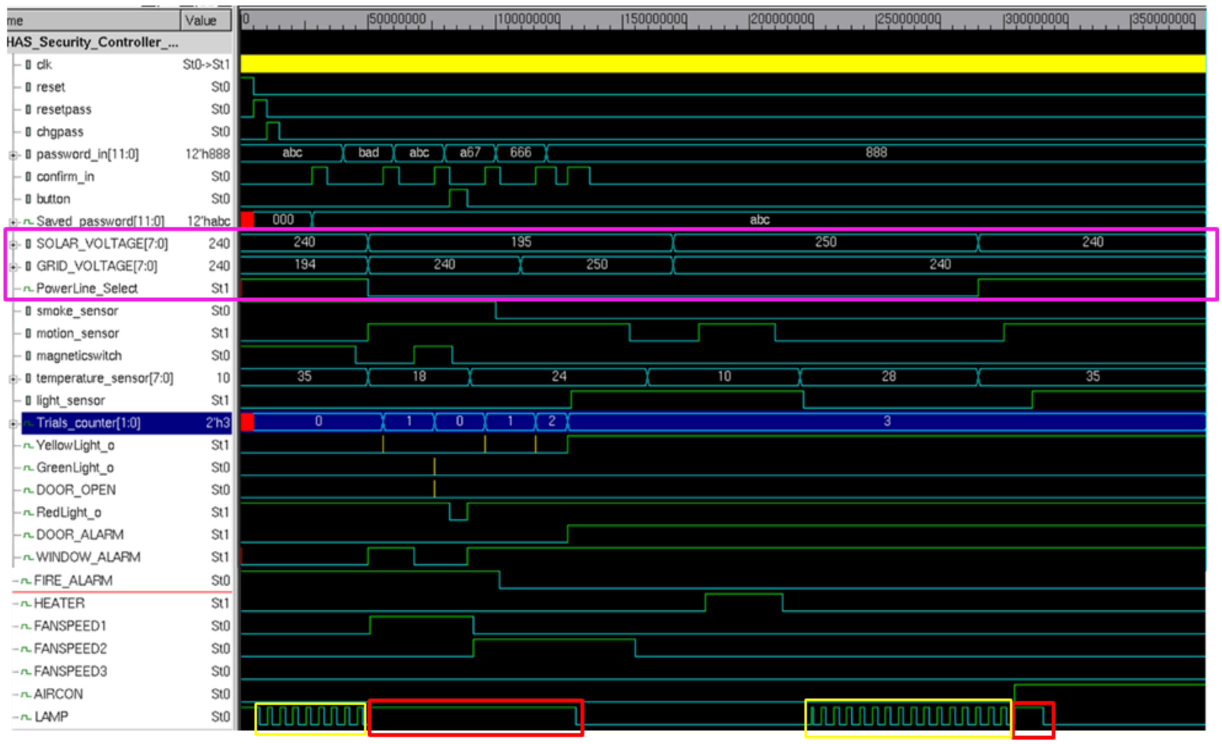

Figure 2: Output waveform of top-level module with 10ns clock period

Table 2 below shows the design metrics obtained in logical synthesis and physical synthesis using same technology library. The total area and total power consumption had been successfully optimized lower at physical synthesis phases. Total power consumption is contributed by cell leakage power and dynamic power. The cell leakage power of the final layout is 3.06µW which is 0.31µW lower as compared to the logical synthesis stage. Total dynamic power obtained in physical synthesis is 62.55µW which is 4.67µW lower than the power obtained in DC Compiler. The final layout of the design is shown in Figure 3.

Table 2: Summary of the performance report in logical synthesis and physical synthesis

Design Metrics	Logical Synthesis	Physical Synthesis
Timing Slack (ns)	1.88	1.95
Total Power (µW)	70.59	65.61
Total Area (µm^2)	664.51	662.44

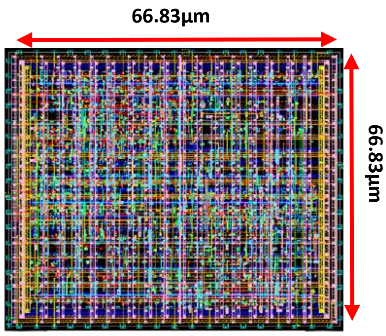

Figure 3: Final Layout of Automated Home System Controller

4. Conclusion

In this project, a small and compact automated home controller with low power is successfully developed using ASIC implementation, whereby each integrated system functioned correctly based on the respective inputs. This controller can be further integrated with other systems or peripherals to form more complex and compact home controller devices to be more affordable whilst reducing the number of components used for the home system accordingly. More control features and voltage fluctuations detection blocks can be implemented in the system in the future.

Acknowledgement

The authors would like to thank the Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia for its support.

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