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The Design and Implementation of Low Power Full Adder and Multiplier for Digital FIR Filter in 90nm CMOS Technology

Johan Lela Andika[1]*, Siti Hawa Ruslan[1]

[1]Department of Electronic Engineering, Faculty of Electrical and Electronic Engineering,
Universiti Tun Hussein Onn Malaysia, 86400 Parit Raja, Batu Pahat, Johor, MALAYSIA

*Corresponding Author Designation

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Abstract: Digital Finite Impulse Response (FIR) filtering is used to produce digital output by taking digital input. Digital filtering is one of the most powerful tools of digital signal processing. In Very Large-Scale Integration (VLSI) technology the usage of Digital Signal Processor (DSP) in FIR filter plays important role in various signal processing. The aim of this project is to have the best power consumption in the design of FIR filter integrated circuits for reasons of portability, miniaturization, and energy conservation. In this project, the design of adder and multiplier circuits for the FIR filters that have the best power consumption is very critical. A custom full adder utilizing the hybrid method and Vedic multiplier using 90 nm Complementary Metal Oxide Semiconductor (CMOS) technology is proposed. By employing the hybrid full adder (HFA) along with the Vedic algorithm, a 3-tap FIR circuit in direct form structure is designed using Cadence EDA tools. With this method, the number of transistors in the adder and multiplier circuits for the FIR filter circuit is less, thus it improves the power consumption of the system. The power consumption for the 4x4-bit Vedic multiplier is 0.212 mW at a supply voltage of 1.0 V.

Keywords: FIR, Hybrid Full Adder, Vedic Multiplier, Low Power

1. Introduction

Digital signal processing is an important part of electronic devices as a signal is an integral part of the Digital Signal Processor (DSP). A signal is pulse coded with information that needs to be transferred from the source to the destination, and the channel is the medium to do so. During the transmission, some of the data is lost due to the noise present in the channel. FIR filters are widely used in various DSP applications such as audio processing, signal processing, software-defined radio, etc. [1]. Digital filters are used in these applications because the noise can be filtered easily, and FIR filters are employed because of frequency stability and linearity in their phase response [2]. In these applications, the required FIR filter is of large order to meet the stringent frequency specifications [3]. FIR filter

*Corresponding author: sitihawa@uthm.edu.my

circuit can be constructed using a direct-form structure [4]-[5]. In this structure, arithmetic circuits like adders and multipliers with a series of delays are the basic building blocks of FIR filters [6]-[7]. The number of multipliers and adders required for each filter output increases linearly with the filter order [3]. Hence this will lead to an increase in area, power consumption and delay [7]. Therefore, an FIR filter circuit with low power consumption and high speed is really needed and it is very crucial for implementation in very large-scale integration (VLSI) designs [8]. This study proposed an FIR filter circuit using a hybrid full adder (HFA) with a small number of transistors and a Vedic algorithm that will produce fast multiplication and small delay.

2. Literature Review

The Vedic algorithm had been proven in producing a fast multiplier [9]-[12]. Hence engaging a hybrid full adder in the Vedic multiplier will further improve its performance and power consumption.

2.1 Urdhva Tiryagbyham Sutra

The Vedic multiplier utilized Urdhva Tiryagbyham Sutra method to calculate any n x n bit number. The Vedic algorithm met the criterion of a rapid multiplication operation because of the vertically and crosswise multiplication notion, which fitted well with parallel multiplication [13]. As a result, the number of partial products is substantially reduced, resulting in a faster multiplication process. Two 2-bit binary numbers A1A0 and B1B0 are shown in Table 1, to depict the Vedic multiplication process [14].

Table 1: 2x2 bit multiplication using Vedic Mathematics

Step	Pictorial Representation	Equations
1. Multiply LSB	●(A1) ●(A0) ↕ ●(B1) ●(B0)	$P_0 = A_0*B_0$
2. Cross multiply the bit	●(A1) ●(A0) ↙ ↘ ↗ ●(B1) ●(B0)	$C_0P_1 = (A_1*B_0) + (A_0*B_1)$
3. Multiply MSB	●(A1) ●(A0) ↕ ●(B1) ●(B0)	$P_3P_2 = (A_1*B_1) + C_0$

3. Methodology

A Cadence software tool is used in the design of the adder and multiplier circuits for the FIR filter. A 90 nm Complementary Metal Oxide Semiconductor (CMOS) technology is utilized in drawing the schematic circuit and simulating it. The hierarchical approach is implemented in the design process where the circuit is designed to block by block at the transistor level.

3.1 The FIR Filter Circuit

Figure 1 shows the proposed block diagram of a 3-tap FIR filter in a direct-form structure [15]. It consists of multipliers, adders, and delay elements. Three 4x4 bit multipliers are needed in the circuit,

along with two 8-bits adders and two delay elements. Each of these blocks is explained in the next section. In the 3-tap FIR filter, as shown in the figure, the values of h(a), h(b), and h(c) are the coefficients that are used for multiplication. Basic logic gates are also designed, and a hybrid full adder is implemented in the multiplier and adder circuits.

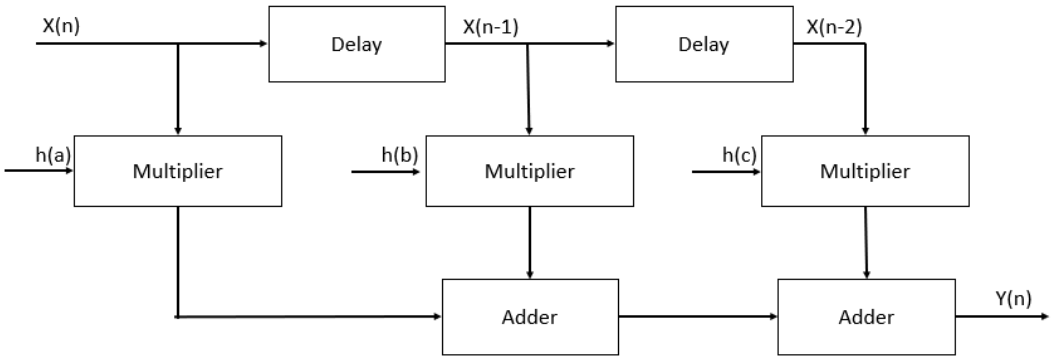

Figure 1: Block diagram of the proposed 3-tap FIR filter

3.2 Hybrid Full Adder

As shown in Figure 2, a 1-bit HFA circuit is built by creating a full adder from three modules. Module I contain a three transistor (3T) XOR circuit, and an inverter. This module produces an XOR-XNOR combination to drive the other two modules. Module II generates a summing circuit (SUM), while Module III generates a carry signal (COUT) [16]. Module I must have a good driving capability and ability to deliver a full swing output because the other two modules rely on the output of the first module. For the 1-bit HFA, a total of 13 transistors (13T) are used. This 1-bit HFA is then cascaded to form a 4-bit HFA in the form of a ripple carry adder and the latter is used to construct an 8-bit adder.

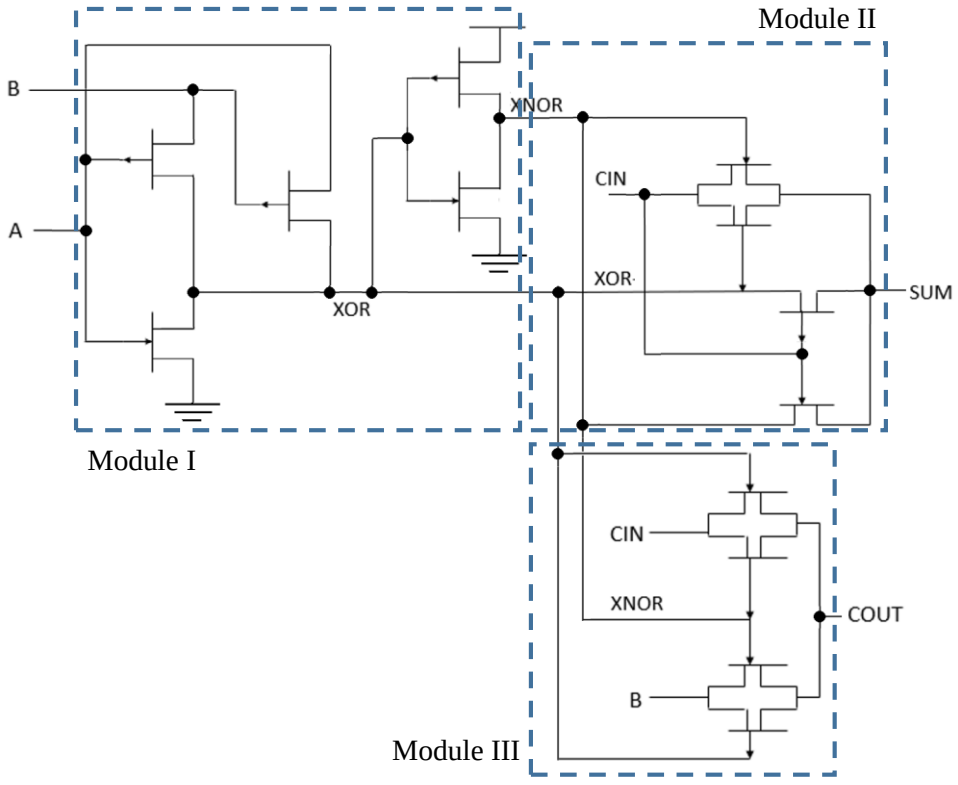

Figure 2: 1-bit hybrid full adder with 13T

3.3 The Proposed Vedic Multiplier

A 2x2 Vedic multiplier is designed first based on Table 1 in order to form a 4x4 Vedic multiplier. The circuit for the 2x2 multiplier is shown in Figure 3. Four AND gates and 2 HFA (FA_1BIT) are used to construct the circuit. The proposed 4x4 bit Vedic multiplier block diagram is presented in Figure 4 and is based on the Urdhva Tiryagbhyam Sutra. This 4x4 bit Vedic multiplier is made up of four 2x2 bit Vedic multipliers and three 4-bit HFAs.

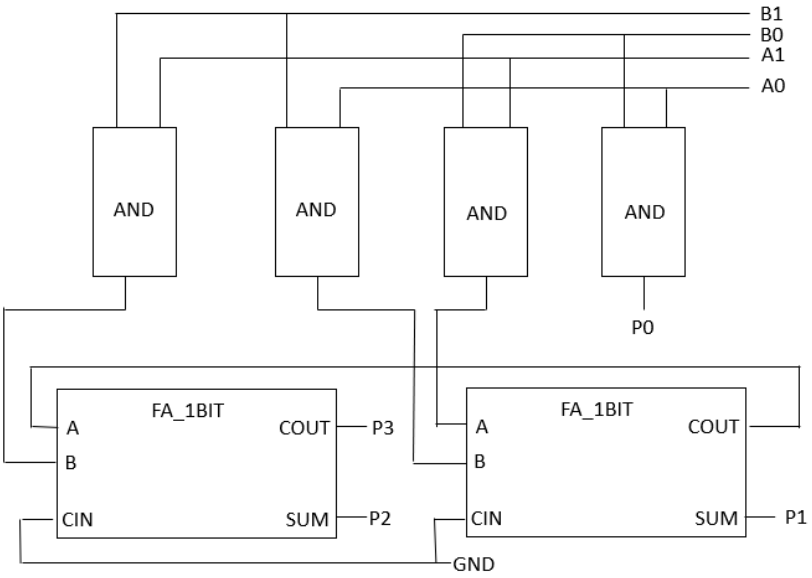

Figure 3: 2x2 bit Vedic multiplier

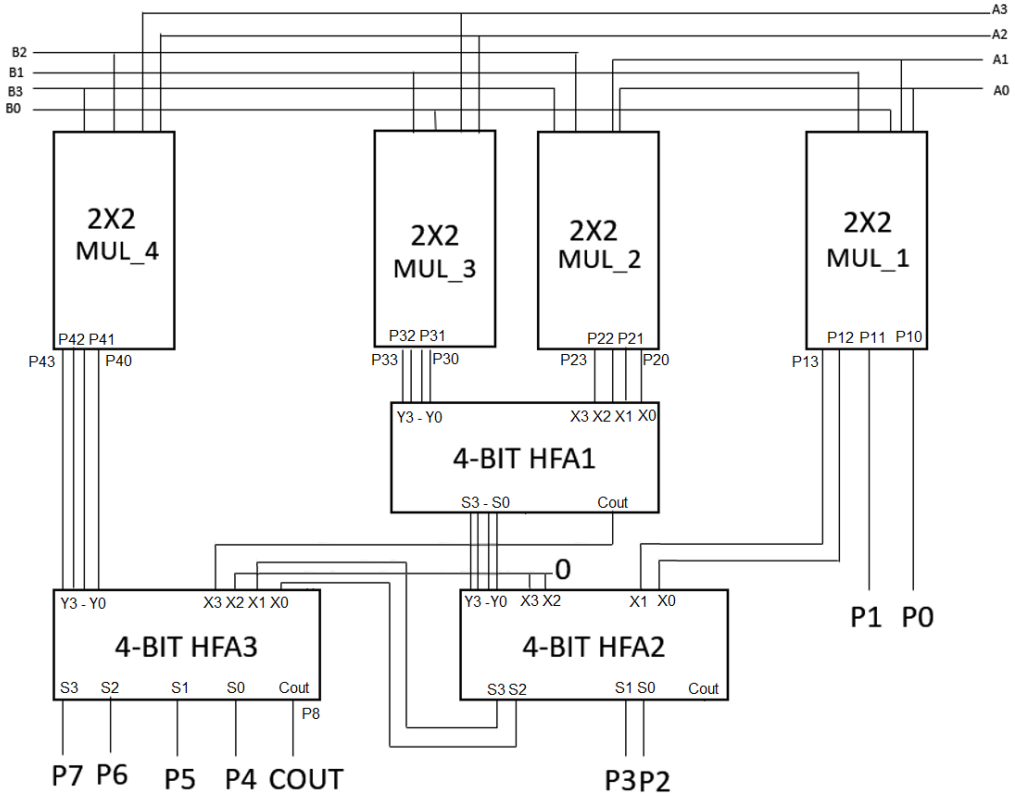

Figure 4: 4x4 bit Vedic multiplier

The multiplication begins with the 2x2 bit Vedic multiplier 1 (MUL1), which produced a product of P13 P12 P11 P10. The direct form of the end bit product of the proposed 4x4 bit Vedic multiplier is P0 and P1 from the 2x2 bit Vedic multiplier 1, while P12 and P13 are sent to 4-bit HFA2 as input X0 and X1 to the HFA2. The multiplication continues until all of the final product's components are completed as shown in Figure 4. In conclusion, the final bit product of the 4x4 bit Vedic multiplier is produced in 2x2 bit Vedic multiplier 1, 4-bit HFA2 and 4-bit HFA3 producing COUT P7 P6 P5 P4 P3 P2 P1 P0.

3.4 The Proposed FIR Circuit

The proposed 3-tap FIR filter is designed using two parallel-in parallel-out (PIPO) registers as the delay elements, three 4x4 bit multipliers and two 8-bit adders. The circuit is depicted in Figure 5. The PIPO is designed using a D flip-flop. In the figure, the first 8-bit adder (HFA1) will add the product from MUL1 and MUL2, while the second 8-bit adder (HFA2) will add the output from MUL3 and the first 8-bit adder (HFA1). The circuit for the adder is shown in Figure 5. The adder is formed using HFA.

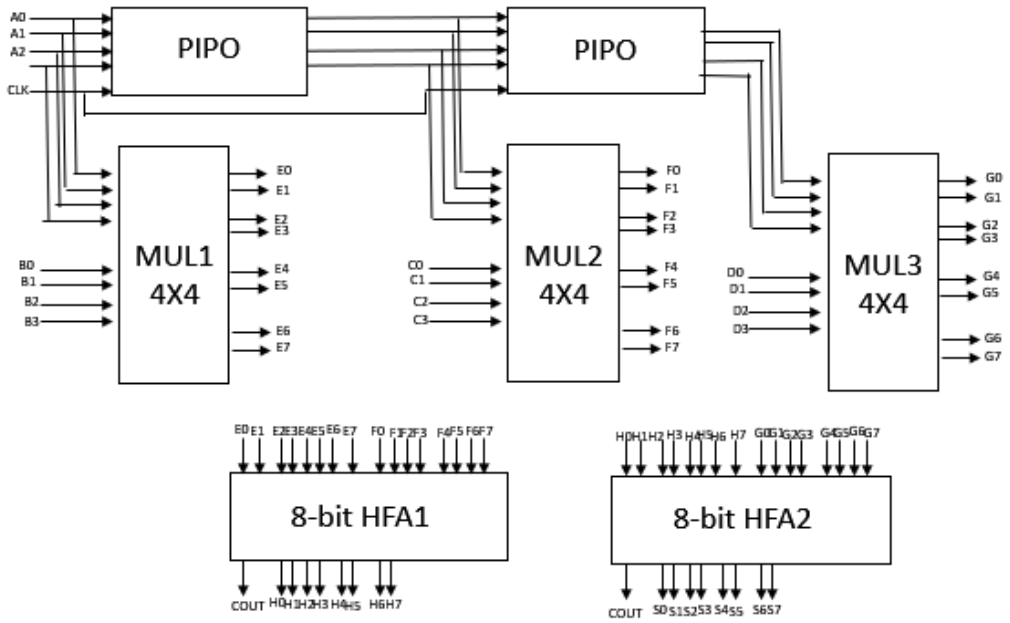

Figure 5: The proposed circuit of the 3-tap FIR filter

4. Result and Discussions

All the circuits are designed using Cadence 90 nm CMOS technology and simulated with a load capacitance of 0.1 pF and supply voltage of 1V.

4.1 Result of Hybrid Full Adder

Figure 6 shows the output simulation for the 1-bit HFA. The result is according to the theoretical values. This means the designed circuit is correct. This 1-bit HFA is then used to form a 4-bit HFA and the result is shown in Figure 7. The result for the 4-bit HFA is according to the theory. Then the 4-bit HFA is used to construct an 8-bit HFA and part of the simulation result is shown in Figure 8. The simulated result of the 8-bit HFA depicted accurate output. This research demonstrated that even when cascaded to generate an 8-bit HFA, the suggested 1-bit 13T HFA can produce a full voltage swing. The 4-bit HFA is used in the 4x4-bit Vedic multiplier, and the 8-bit HFA is used in the proposed FIR filter circuit.

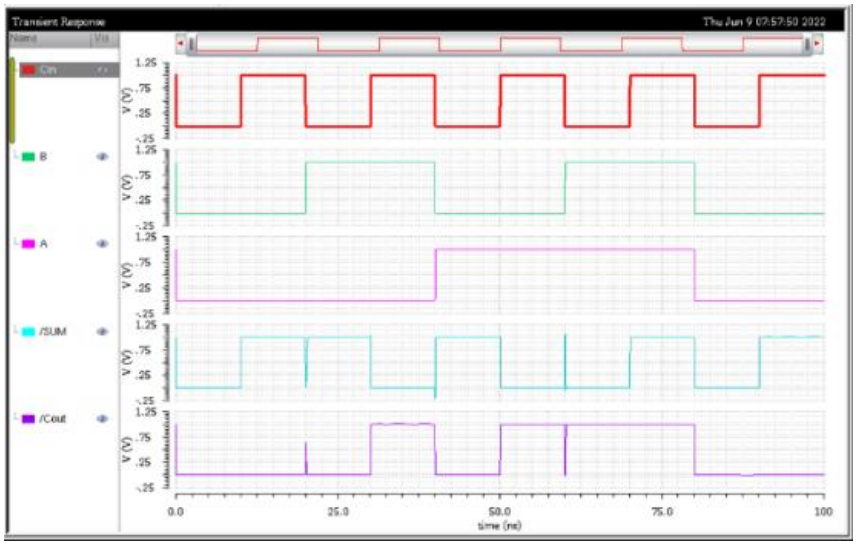

Figure 6: Waveform of 1-bit Hybrid Full Adder

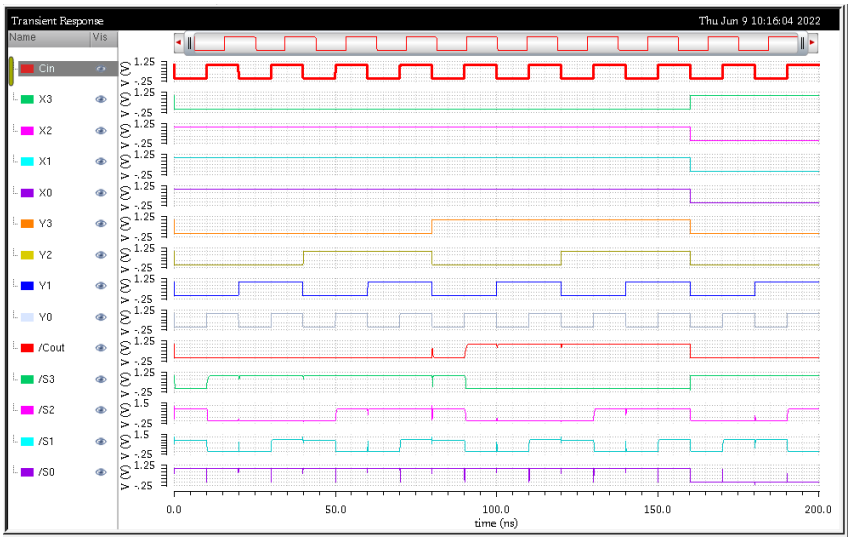

Figure 7: Waveform of 4-bit Hybrid Full Adder

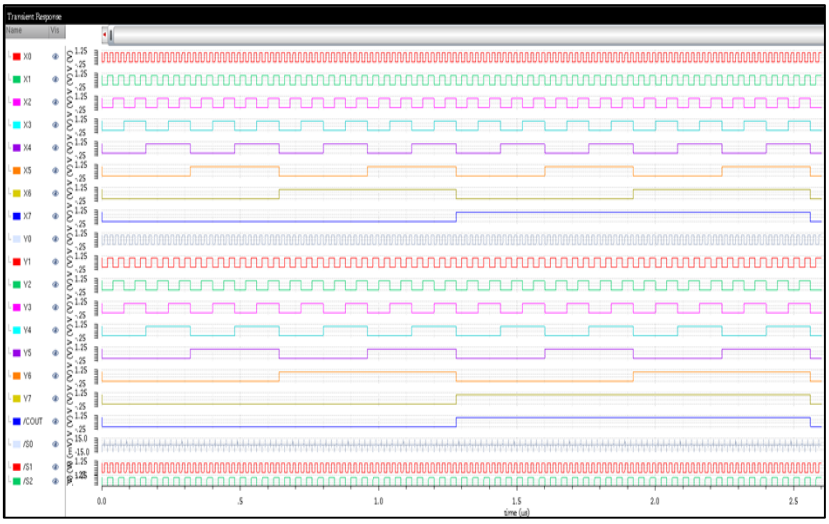

Figure 8: Waveform of 8-bit Hybrid Full Adder

4.2 Result of Vedic Multiplier

The output for the 2x2 bit Vedic multiplier is illustrated in Figure 9. The output waveforms are correct and according to the theoretical value. The 2x2 bit multiplier along with the HFA has then been used in the design of the 4x4 bit Vedic multiplier. The result of the 4x4 bit multiplier is shown in Figure 10. The result reveals that the hybrid full adder and Vedic mathematics had successfully created the 4x4 bit Vedic multiplier with only 1 V of power supply with output having a full voltage swing. The power consumption of the 4x4 bit Vedic multiplier is 0.212 mW.

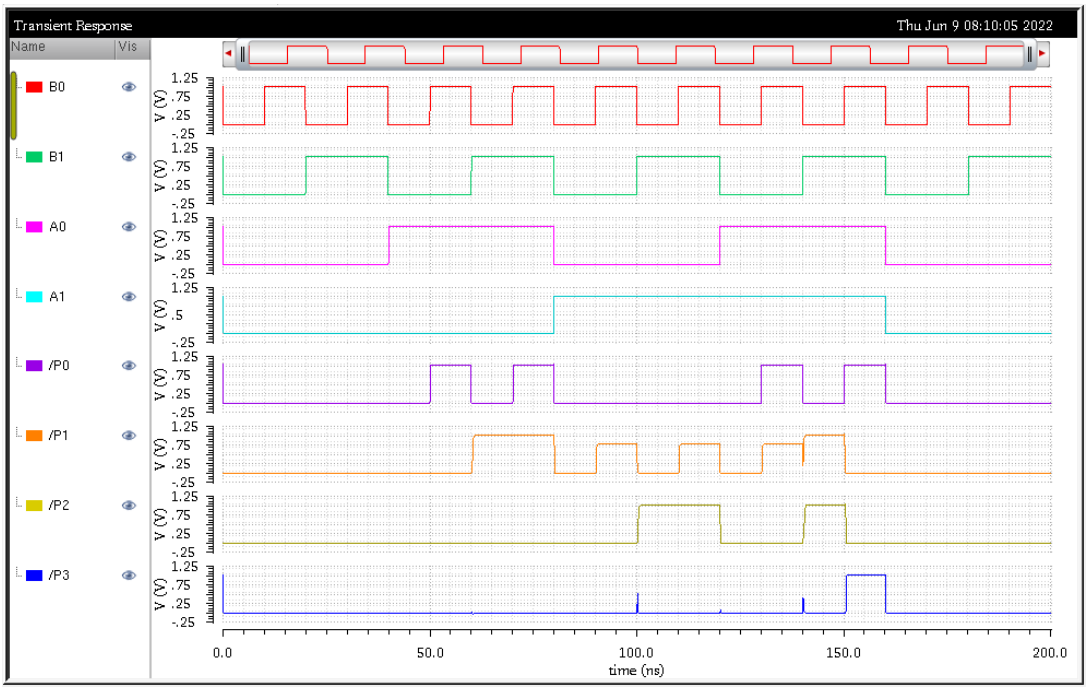

Figure 9: Waveform of 2x2 bit Vedic Multiplier

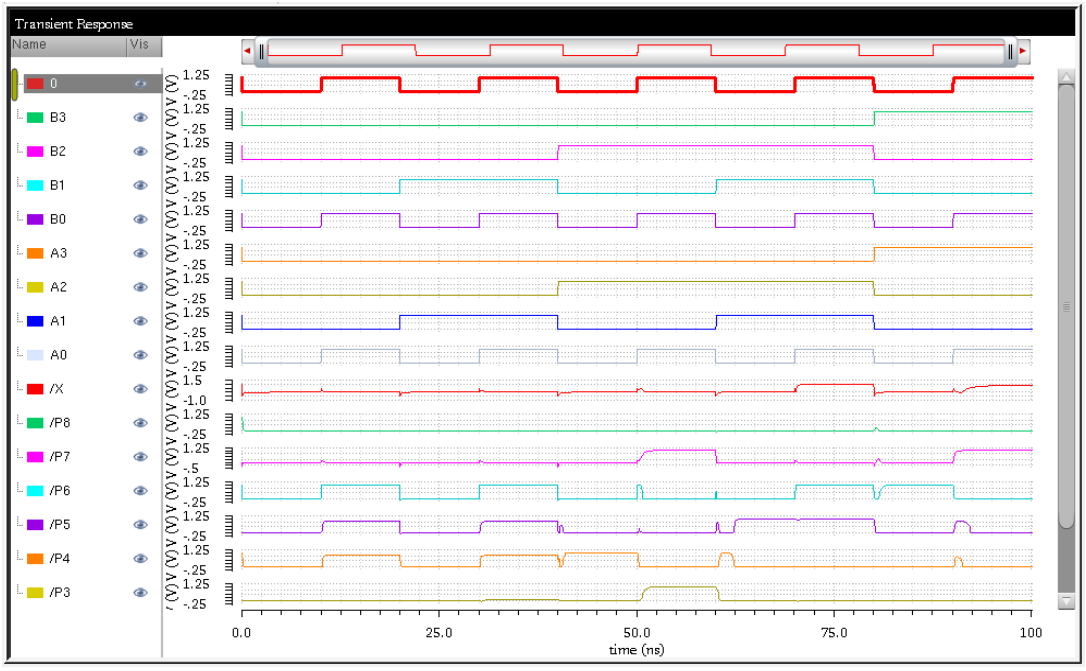

Figure 10: Waveform of 4x4 bit Vedic Multiplier

4.3 FIR Filter Circuit

Figure 11 shows the 3-tap FIR filter circuit that has been designed for this project. It consists of the adders, multipliers, and delay blocks as all of these blocks represented the FIR filter structure in direct form. The adders and multipliers had been shown in the previous section are working perfectly according to the theory. The delay blocks which are the shift register are also working as they should be as delay input to move the data input to another block.

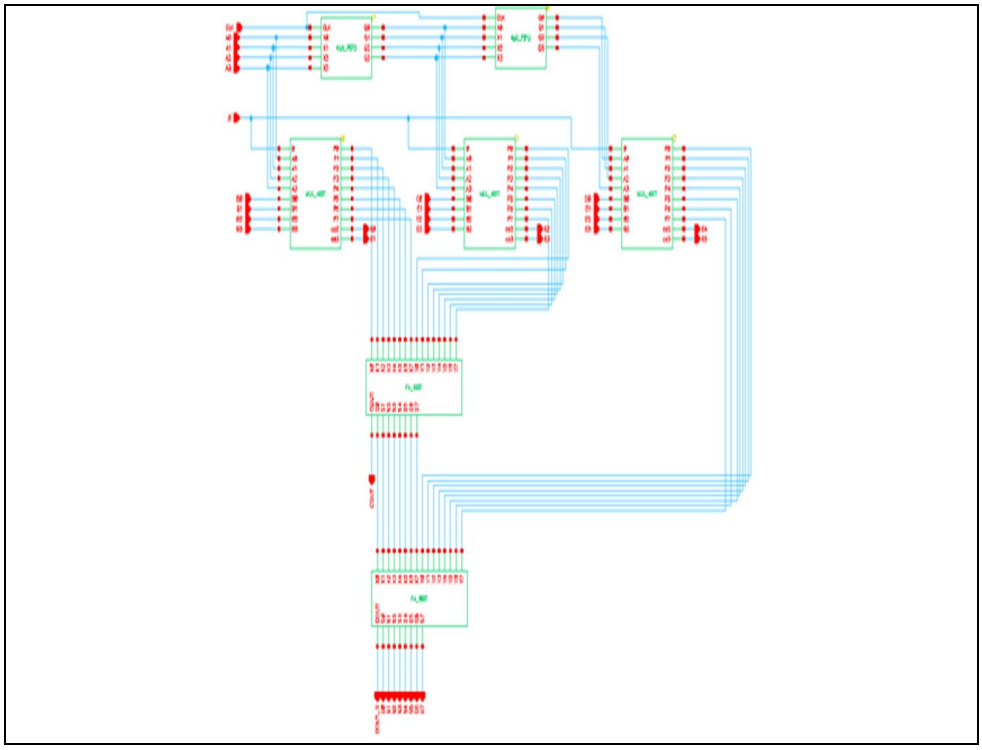

Figure 11: 3 tap 4-bit FIR filter schematic

The FIR filter simulated waveforms are depicted in Figure 12. The output is correct and according to the theoretical output, as illustrated in Table 2 and Table 3. The result reveals that the HFA, Vedic multiplier and PIPO used had successfully created the 3-tap 4-bit FIR filter. With only 1 V of the voltage supply, the 3-tap 4-bit FIR filter performs perfectly.

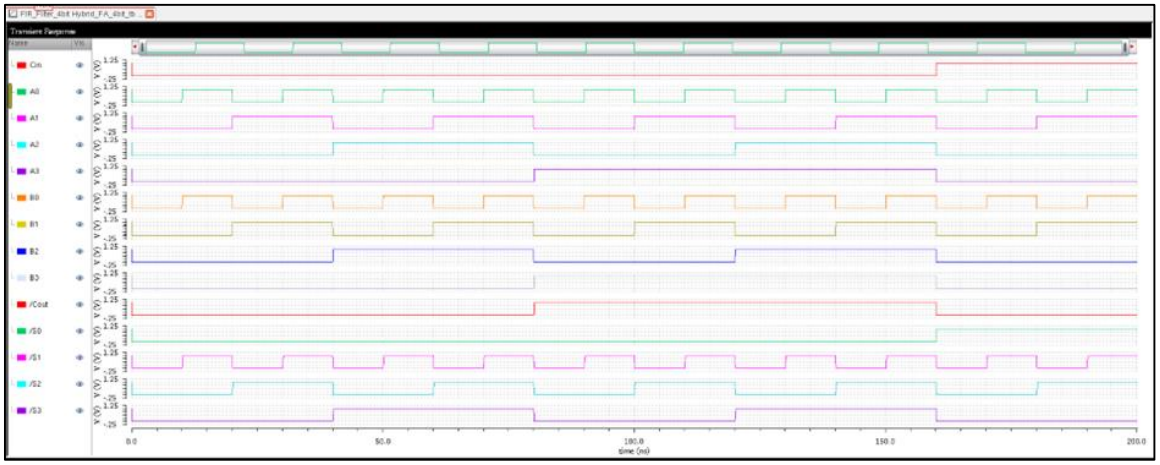

Figure 12: 3-tap 4-bit FIR filter simulation result

Table 2: Truth table for 1st tap & 2nd tap FIR filter

INPUT									OUTPUT																					
	X(m)				X(n)					1st Vedic Multiplier								2nd Vedic Multiplier								1st 8-bit Full Adder							
x	B3	B2	B1	B0	A3	A2	A1	A0	CIN	P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0	COUT	S7	S6	S5	S4	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	1	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0
0	0	1	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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0	1	0	1	0	1	0	1	0	0	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0
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1	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	0	1	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1

Table 3: Truth table for 3rd tap FIR filter

INPUT									OUTPUT																					
	X(m)				X(n)					1st 8-bit Full Adder								3rd Vedic Multiplier								2nd 8-bit Full Adder							
x	B3	B2	B1	B0	A3	A2	A1	A0	CIN	P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0	COUT	S7	S6	S5	S4	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
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1	1	1	1	1	1	1	1	1	0	0	1	0	1	0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	1	1	1	1	0	0

5. Conclusion

A low-power, high-speed, 4x4 bit multiplier has been successfully constructed utilising the Vedic algorithm technique. This project includes the use of a 13T hybrid full adder (HFA). The HFA operation had been tested throughout this project as it is used in the design of 4-bit and 8-bit HFA. When compared to a conventional circuit of 28T 1-bit full adder with an array multiplier, the combination of the HFA and Vedic mathematics algorithm saves 1140 transistors in a 4x4 bit multiplier. Meanwhile, with a 1V power supply, the result of 4x4 bit multiplication was produced in 365 ps and the power consumption of this multiplier is only 0.212 mW. Hence these adders and multipliers will result in a low-power FIR filter.

Acknowledgement

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