Evolution in Electrical and Electronic Engineering Vol. 1 No. 1 (2020) 145 -152

EEEE

Homepage: http://penerbit.uthm.edu.my/ojs/index.php/eeee
e-ISSN : 2756-8458

Performance Optimization of Face Detection Algorithm

Cheang Kah Ying[1], **Siti Hawa Ruslan**[1*]

[1]Faculty of Electrical and Electronic Engineering,
Universiti Tun Hussein Onn Malaysia, 86400 Parit Raja, Batu Pahat, Johor, MALAYSIA

DOI: https://doi.org/10.30880/eeee.2020.01.01.017
Received 13 August 2020; Accepted 06 September 2020; Available online 30 October 2020

Abstract: Human face detection is known as one of the most concerned topics in numerous fields such as monitoring and surveillance system. In today's era, the existed face detection system is needed to be modified and optimized to adapt the changing demands. In this study, the face detection system with Viola-Jones algorithm had been used, modified, and optimized. The compilation of the optimized face detection system is conducted in Very High Speed Integrated Circuit Hardware Description (VHDL) language by using Quartus Prime 15.1 Lite Edition software. The new optimized face detection system is applied on the Altera DE2-115 Development and Education board. Several performance measurements such as power consumption, computing frequency and accuracy are carried out to examine the performance of the new optimized and implemented structure. To evaluate the accuracy of the new face detection system, the results of the measurements were compared to the results of the original face detection system. The obtained results had shown some improvement on the performance of the face detection system.

Keywords: Face Detection, Viola-Jones Algorithm, Low Power

1. Introduction

In recent years, human faces processing become of broad interest in the image processing field. Human face processing is an important aspect in numerous applications for various domains such as human computer interaction, monitoring and surveillance system. In general, an ordinary face processing system comprises four stages which are face detection, face recognition, face tracking and face rendering.

Face detection is described as the process of detecting the presence of human faces from other objects and the background. If there is any occurence of face in the given arbitrary image, then the image location and spatial location for each face is returned [1]. Basically, face detection is the fundamental step in the face processing system. Currently, the embedded face detection system with the function of face-priority autofocus (AF) has been implemented in recent digital camera terminology. Face detection system is also used for the purpose of automated photo tagging in the social network system such as Facebook [2].

*Corresponding author: sitihawa@uthm.edu.my

Over the past few years, several face detection algorithms have been developed to determine the appearance of human faces in an image regardless the locations, numbers, sizes, and orientations. In this study, a face detection system is proposed by adapting Viola Jones face detecting algorithm [3] and the performance of the Viola Jones algorithm is optimized. Viola-Jones face detection algorithm is one of the best algorithms over the years [4]. By implementing this algorithm, a face detection system can be optimized, and thus improve its performance.

1.1 Problem statement and objectives

The development of computerized face detection system which equals the human capability is still a challenge today. This is because of the features of human faces are non-rigid in face alignment and have great differences in skin colour, texture, shape and size [5]. There are many challenges in the implementation of face detection algorithm that emulate the functionality of human eyes. Still, the performance of the automated face detection system unsurpassed the accuracy and rapidity of the human ability [6]. Majority of the current face detection system in the devices is run by using software [7]. The implemented algorithm may influence the performance of the face detection system where the complex algorithm can lead a better face detection performance. However, huge processing power is required when complex algorithm is implemented in the software on the conventional microprocessor. To overcome the problem stated, hardware implementation of face detection system on field-programmable gate array (FPGA) is suggested where the compute-intensive algorithms can be designed through dedicated hardware cores and the other parts of the system can be operated in software through the embedded processor [8]. Hence, the objectives of this study are to reduce the power consumption of the implemented face detection system, and to implement an optimized face detection algorithm on FPGA.

2. Methodology

This section describes the methods and process used to optimize the performance of the face detection algorithm. The hardware implementation of face detection algorithm on FPGA board along with the software implementation are described.

2.1 Hardware implementation

To evaluate the performance of the optimized face detection system, Altera DE2-115 Development and Education Board is used to implement the optimized face detection system to analyze the captured images from the OV7670 VGA camera module. A generic Video Graphics Array (VGA) monitor is used to display the face detection results. OV7670 VGA camera module is implemented to process 640 x 480 resolutions of captured images and transfer the output data in RGB565 format at 30 frames per second. Moreover, Altera DE2-115 Development and Education Board is selected as the platform because it offers a lower cost, and lower power. It equips huge supply of logic with 114,480 logic elements, 3888 Kbits of embedded memory and digital signal processor (DSP) capabilities [9]. The VGA monitor is used to display the results of the processing steps in the optimized face detection system in the size of 320 x 240 images.

Figure 1 illustrates the complete connection of the implemented face detection system. The optimized face detection system is compiled using Quartus Prime 15.1 Lite Edition software and programmed to the Altera DE2-115 board. Furthermore, the VGA monitor is connected to the DE2-115 board via VGA cable and the OV7670 camera module is connected to the DE2-115 board through the General Purpose Input/Output (GPIO) pins.

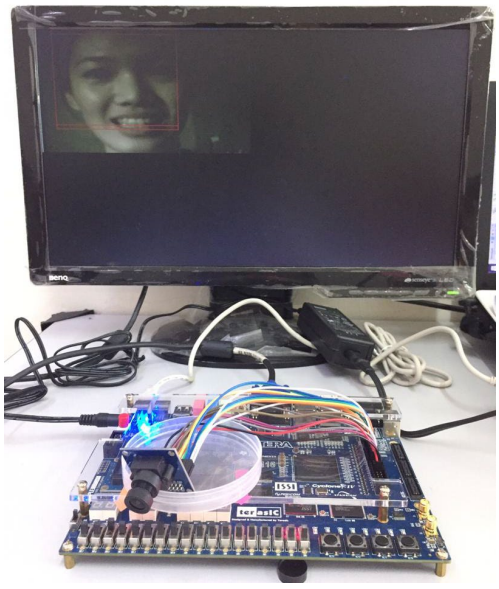

Figure 1: Project hardware setup

2.2 Software implementation

In this study, the source code of the FPGA based implementation of Viola-Jones algorithm from the researchers in [10] is applied and modified to optimize the efficiency. The results of the optimization on the source code is compared with the results of the original coding. In order to evaluate the performance of the face detection system, the real time captured images data from the OV7670 camera module is used to test the functionality of the code. The top-level design of this face detection system involves numerous parts which include top level control panel, camera drivers, images processing stages and result display. The top-level control is entitled to control all the components in the top-level design. In addition, the image processing stages consists of integral image generator, sub-window kernel and face box component. Figure 2 explains the structure of the top-level design.

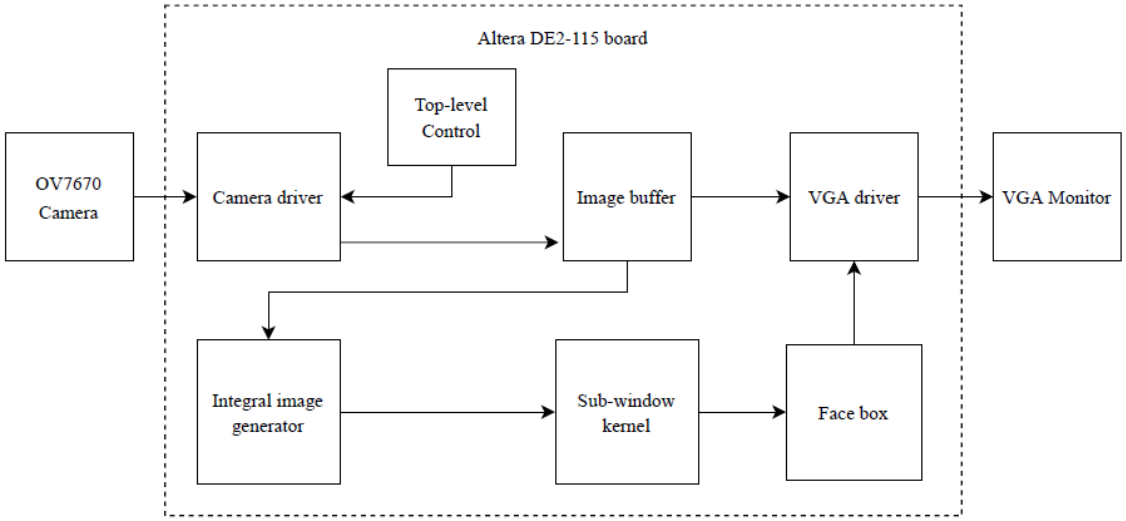

Figure 2: Top-level design

In first step, the top-level control will allow the camera driver to capture new images and drive the captured images data into the image buffer. Next, the image buffer will pass the images data to the

image processing stages and display the captured images on the VGA monitor synchronously. In the image processing stage, the integral image generator will generate an integral image in the size of 39 x 59 pixels. Then, the generated integral images will be analyzed in 16 parallel sub-window kernels and scanned for the existed human faces in the images. Once the scanner completed the processing steps, the system will indicate the detected faces in the original captured image by using the red bounding box which is generated from face box component.

In order to create the integral images, the conversion of images data from 12 bits Red Green Blue (RGB) colour model to 8 bits grayscale is needed. In integral image generator, the accumulators and repetitive computation are implemented to generate the resultant integral image where the accumulator is developed to calculate the sum of the converted grayscale data at the latest location of (x,y).

In the sub-window kernel, a number of 25 strong stages of the cascade classifier is implemented whereas the feature evaluation is conducted based on the accumulated values from the feature calculation in a sub-window with the size of 24 x 24 pixels. Yet, the values from feature evaluation will be compared with all 25 strong classification stages. When the compared values is less than thresholds, the sub-window will determine that no human face is detected. Throughout all the classification stages, the sub-window will determine that human face is detected without non-human faces.

Furthermore, face box is designed to store the results of the face detection and indicate the occurrence of human faces in the captured image frame. Based on the detection results, the face box will indicate the detected human faces by putting a red rectangular box around the faces. Figure 3 shows the functionality of the face box.

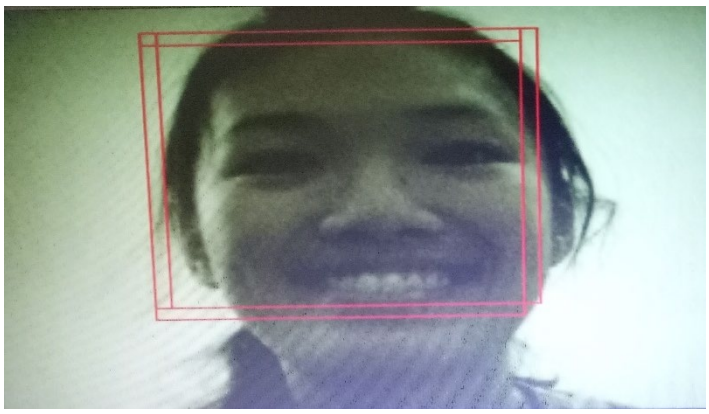

Figure 3: Functionality of face box

2.3 Optimization techniques

To improve the performance of the face detection system implemented in this study with the aim of enhancing the power efficiency and computing frequency of the system, modification had been done to the original face detection system without compromising the accuracy of the face detection. In order to reduce the power dissipation of the implemented face detection system, the cascade classification stages are reduced. In this study, the number of the strong classification stages is reduced from 25 to 23 whereas the number of the weak node counter is reduced from 2914 to 2900. The number of the weak node counter is relevant to the strong cascade classifier. By reducing the cascade classification stages, the total logic elements of the system will be reduced too.

Likewise, the decrease of the total number of logic elements will lead to the decline of the power consumption of the face detection system. The power consumption of the optimized face detection system will be measured by using the PowerPlay Power Analyzer tool in the Quartus Prime 15.1 Lite Edition software and compared with the power consumption of the original face detection system. Figure 4 illustrates the strong classification stages after reduction.

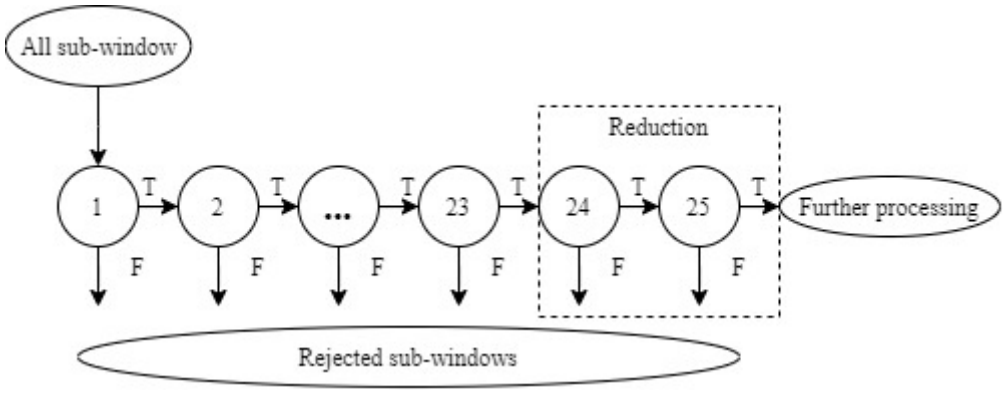

Figure 4: Reduction on cascade strong classifier stages

Besides, the optimization tools built in Quartus Prime are used to enhance the performance of the face detection system in the terms of power efficiency and the computing frequency. Firstly, the optimization mode in the Quartus Prime had been modified to power optimization mode which will minimize the power dissipation of the design through netlist optimizations. To improve the computing frequency of the face detection system, the advanced fitter settings is modified in Quartus Prime.

By changing the setting of "Logic Cell Insertion" to Auto, the performance of the design can be enhanced with a nominal compilation time increment. The fitters in design can be optimized to meet the maximum delay timing requirement as turning on the normal compilation for the "Optimize Timing" settings. The automatic insertion of pipeline for asynchronous signals is applied in order to improve the performance of the circuit which is useful for removal timing and failing recovery. By performing the optimization of physical synthesis on the combinational logic during fitting, the performance of the design can be improved.

3. Results and Discussion

This section will describe the results and analysis for the implementation of optimized face detection system. The performance of the optimized face detection system in terms of power consumption, computing frequency and accuracy will be discussed. After that, this section compares the performance of the original face detection system and the optimized face detection system.

3.1 Results

The compilation of the optimized face detection system is performed in Quartus Prime 15.1 Lite Edition software by using ASUS A550L with Intel Core i5 4200U 1.60GHz. The implementation of the optimized face detection system is carried out on the Altera DE2-115 development and education board.

To evaluate the power consumed by the optimized face detection system, PowerPlay Power Analyzer tool in the Quartus Prime 15.1 Lite Edition software is used. In the settings of the PowerPlay Power Analyzer tool, the junction and ambient temperatures are 25 °C by the default board. In addition, the toggle rate for the input I/O signal and the remaining signals are set to 50%. The measured results is compared with the results of the original face detection system.

Table 1: Comparison table for the power consumption

Power dissipation	Original system	Optimized system	Unit or Dimension
Total thermal power	2497.39	2417.00	milliWatts (mW)

Core dynamic thermal power	2300.88	2220.90	milliWatts (mW)
Core static thermal power	113.59	113.19	milliWatts (mW)
I/O thermal power	82.92	82.92	milliWatts (mW)

Based on result tabulated in Table 1, the comparative analysis of the power consumption for the original face detection system and the optimized face detection system is shown. After implementing optimization, the power consumption of the face detection system is improved considerably. Through the implemented optimization techniques, the total thermal power dissipation has dropped by 3.22 %. Besides, the core dynamic thermal power dissipation decreased by 3.48 % and the core static thermal power declined by 0.35%. However, the value of the I/O thermal power dissipation remain constant after optimization.

To examine the computing frequency of the optimized face detection system, TimeQuest Timing Analyzer in the Quartus Prime 15.1 Lite Edition software is used. In this study, the maximum frequency of the top-level control and sub-window kernel will be focused. The timing analysis results is compared with the results of the original face detection system.

Table 2: Comparison table for the timing analysis

Timing results	Original system	Optimized system	Unit or Dimension
Maximum frequency	42.17	44.82	MegaHertz (MHz)
Longest data delay	23.71	22.31	Nanosecond (ns)

Table 2 had shown the comparison of the timing analysis for the original face detection system and the optimized face detection system. Noticeably, the improvement of the timing performance of the face detection system is observed by implementing the optimization techniques. According to Table 2, the maximum frequency at the top-level control and sub-window kernel is increased by 6.28 %. Likewise, the longest data delay is determined with regard to the clock timing. The longest delay is noticed to have declined by 5.90 %.

In order to measure the functionality of the optimized face detection system, the accuracy of the detection results is analyzed. The accuracy testing is carried out on the hardware implementation where the optimized face detection system with Viola-Jones algorithm is implemented. During the accuracy testing, ten measurements are conducted by using ten different data samples as the input of the face detection. The accuracy testing is conducted under the same environment with the normal light exposure. The verification of the testing included the results of the number of detected human faces in the input images and the comparative analysis between the original coding and the modified coding.

Table 3 shows the analysis of the accuracy of the detection results for the original face detection system and the optimized face detection system. Significantly, the accuracy of the optimized face detection system did not affected by the reduction of the cascade classification stages. In addition, the detection results of the optimized face detection system for both data samples 8 and 10 are better than the detection results of the original face detection results.

Table 3: Comparison table for the accuracy of detection results

Data sample	Total number of faces	[Original system] Number of detected faces	[Optimized system] Number of detected faces
1	1	1	1

2	2	2	2
3	1	1	1
4	2	2	2
5	3	3	3
6	5	5	5
7	6	6	6
8	8	7	8
9	10	10	10
10	15	14	15

3.2 Discussions

The results for the power measurement had proven that the reduction of cascade stages helped to decrease the power consumption by decreasing the total combinational logic whereas the power optimization mode in Quartus Prime helped to reduce dynamic thermal power effectively. Yet, the unchanged I/O thermal power dissipation might be due to the unmodified number of input and output in this face detection system. Moreover, the results of the timing analysis had proven the enhancement of computing frequency in this optimized face detection system. A significant improvement is achieved by the fitters optimization which helped the design to meet the maximum delay timing. Additionally, the accuracy of detection results show the enhancement where the reduction of cascade classifier stages helped to increase the rate of the true positive for the face detection. However, the occurrence of false positive is observed which is might be due to the limitation of the OV7670 camera module. The capture resolution of OV7670 is affected by the intensity of light in the surroundings. Therefore, the performance of the face detection system is relying on the functionality of the camera and also the light level of the environment.

4. Conclusion

In conclusion, the performance optimization is implemented successfully on the original face detection system with the Viola-Jones algorithm. The improvement for the performance of the face detection system is achieved by applying several optimization techniques. The results of the modified face detection system have been obtained and verified by comparing with results of the original face detection system. In the software implementation, the results obtained show the enhancement for the performance of the optimized face detection system which is in terms of power consumption and the computing frequency. The optimized face detection system is implemented on Altera DE2-115 Development and Education board efficiently. The accuracy of the optimized face detection system is proven by the results of the hardware implementation. In order to enhance further the performance of the system, the implementation of pipelining is suggested to be carried out in future work. Likewise, the simplification and modification of the coding for the face detection system is recommended for the future development. Nevertheless, the hardware implementation of the face detection system can be enhanced by using a better resolutions camera.

Acknowledgement

The authors would like to sincerely appreciate the facility used in this study Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia.

References

[1] M. H. Yang, D. J. Kriegman, and N. Ahuja, "Detecting faces in images: A survey," IEEE Trans. Pattern Anal. Mach. Intell., vol. 24, no. 1, pp. 34–58, 2002

[2] S. Zafeiriou, C. Zhang, and Z. Zhang, "A survey on face detection in the wild: Past, present and future," Comput. Vis. Image Underst., vol. 138, pp. 1–24, 2015

[3] P. Viola and M. Jones, "Robust real-time face detection," in Proceedings Eighth IEEE International Conference on Computer Vision. ICCV 2001, vol. 2, no. 2, pp. 747–747, 2004

[4] K. Aashish and A. Vijayalakshmi, "Comparison of Viola-Jones and Kanade-Lucas-Tomasi face detection algorithms," Orient. J. Comput. Sci. Technol., vol. 10, no. 1, pp. 151–159, 2017

[5] A. El Maghraby, M. Abdalla, O. Enany, and M. Y. El Nahas, "Detect and analyze face parts information using Viola- Jones and geometric approaches," Int. J. Comput. Appl., vol. 101, no. 3, pp. 23–28, 2014

[6] A. R. Bhatia, N. M. Patel, and N. C. Chauhan, "Parallel implementation of face detection algorithm on GPU," Proc. 2016 2nd Int. Conf. Next Gener. Comput. Technol., pp. 674–677, October 2017

[7] D. Han, J. Choi, J. Cho, and D. Kwak, "Design and VLSI implementation of high-performance face-detection engine for mobile applications," Dig. Tech. Pap. - IEEE Int. Conf. Consum. Electron., n, pp. 705–706, 2011

[8] S. V. Dharan, M. Khalil-Hani, and N. Shaikh-Husin, "Hardware acceleration of a face detection system on FPGA", IEEE Student Conf. Res. Dev. SCOReD 2015, pp. 283–288, 2015

[9] "Terasic - DE main boards - Cyclone - Altera DE2-115 development and education board." [Online]. Available: https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=502&PartNo=3. [Accessed: 15-Jul-2020]

[10] P. Irgens, C. Bader, T. Lé, D. Saxena, and C. Ababei, "An efficient and cost effective FPGA based implementation of the Viola-Jones face detection algorithm," HardwareX, vol. 1, pp. 68–75, 2017