Evolution in Electrical and Electronic Engineering Vol. 3 No. 1 (2022) 037-043

EEEE

Homepage: http://publisher.uthm.edu.my/periodicals/index.php/eeee
e-ISSN : 2756-8458

The Design and Implementation of Low-Power 4-bit Reversible Multiplier

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DOI: https://doi.org/10.30880/eeee.2022.03.01.005
Received 31 January 2022; Accepted 09 March 2022; Available online 30 June 2022

Abstract: Most processors operating using irreversible logic had wasted a significant amount of energy. Most of this is coming while performing the arithmetic operation and one of the operations is the multiplier. A fast multiplier is needed since slow multiplication can affect the performance of the processors. Hence, reversible logic can be implemented to solve the energy wastage and performance issues in the multiplier. Reversible logic has been brought out to be an optimistic computing model having applications in low power Complementary Metal Oxide Semiconductor (CMOS), nanotechnology, quantum computing, and deoxyribonucleic acid (DNA) computing. This project has investigated the power consumption and speed efficiency of a 4-bit reversible multiplier. The multiplier is based on the Wallace architecture and uses the Peres gate as the reversible logic gate. The circuit is designed using Mentor Graphics with 130 nm and 180 nm CMOS technology and the supply voltage is at 1 V and 1.2 V. It is found that the power consumption for the reversible multiplier circuit using 130 nm and 1 V is 583.35 µW while for 1.2 V, it is 1.0853 mW. As for the speed, the reversible multiplier is 27.5% faster than the conventional multiplier where the average delay is 69.48 ps. In conclusion, it can be said that a reversible multiplier is better than a conventional multiplier.

Keywords: Reversible Logic Gate, Reversible Logic Circuit, Reversible Multiplier, Power Consumption

1. Introduction

The multiplication operation plays an important role in conventionally used digital circuit systems such as for digital signal processing applications and microprocessors, as it dictates the execution time of the digital system operations [1]. Most of these processors use irreversible logic. Irreversible logic is defined as a logic operation that will erase bits of information every time logic operations were performed. The information loss occurred in irreversible logic dissipated heat which can be calculated as kTln2 where T is the absolute temperature while k is the Boltzmann constant (1.3807*10-23J/K) [2], [3].

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It has been proven that the reversible logic has zero energy loss [3]. Reversible logic can increase the operating speed with minimal power consumption. Each input and output of reversible logic design have a unique pattern where inputs were derived from their respective outputs, resulting in making back computation in reversible circuits, which greatly reduces the risk of information loss [1], [4]. Examples of reversible gates include Fredkin Gate, Peres Gate and Feynman Gate [5]. Figure 1 shows the block diagram of the reversible logic gates respectively.

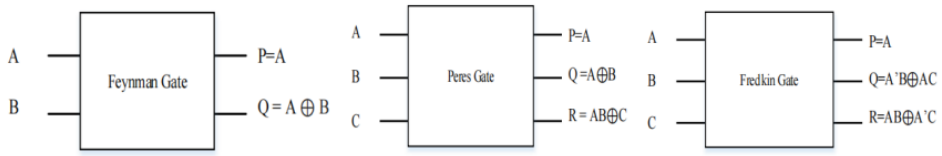

Figure 1: The block diagram of the reversible logic gates [2]

2. Research Methodology

2.1 Design of Half Adder

Half adder is an adder with two inputs of A and B and produces two outputs of SUM and Cout. The equations for the output SUM and C_{out} are shown in *Eq. 1* and *Eq. 2*.

$$SUM = A \oplus B \qquad \textit{Eq. 1}$$

$$C_{out} = AB \qquad \textit{Eq. 2}$$

By referencing the equations of the outputs of SUM and C_{out}, the hierarchical design method is used to design the half adder in the CMOS technique as shown in Figure 2.

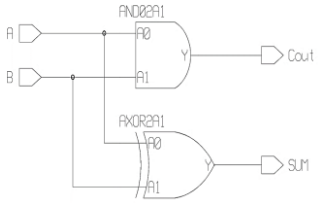

Figure 2: The schematic design for half adder

2.2 Design of Full Adder

A full adder is an adder with 3 inputs of A, B and C which produces two outputs of SUM and C_{out}. The equations for the output SUM and C_{out} are expressed in equations Eq. 3 and Eq. 4.

$$SUM = C_{in} \oplus (A \oplus B) \qquad \textit{Eq. 3}$$

$$C_{out} = AB + (A \oplus B)C_{in} \qquad \textit{Eq. 4}$$

The hierarchical design method is used to design the full adder in the CMOS technique based on the outputs of SUM and C_{out} and the circuit is illustrated in Figure 3.

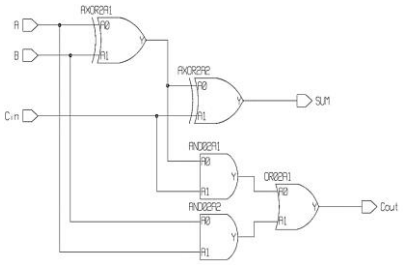

Figure 3: the schematic design for the full adder

2.3 Design of Peres Gate

Peres gate is a 3*3 reversible gate with an input vector of A, B and C and output vector P, Q and R. The outputs can be expressed by equations *Eq. 5*, *Eq. 6* and *Eq. 7*.

$$P = A \quad \textit{Eq. 5}$$
$$Q = A \oplus B \quad \textit{Eq. 6}$$
$$R = AB \oplus C \quad \textit{Eq. 7}$$

From the output expression, the Peres gate can be designed in CMOS by using the XOR gate and AND gate and the circuit is as shown in Figure 4.

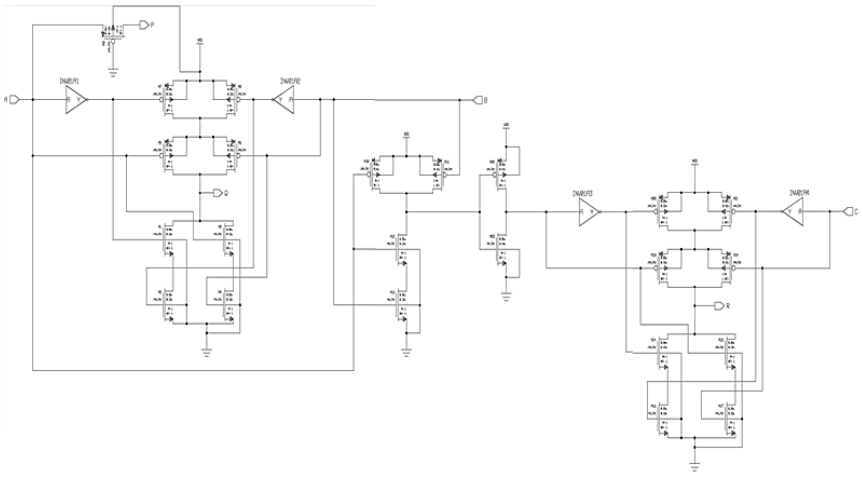

Figure 4: CMOS realisation of Peres gate

2.4 Design of Peres Full Adder Gate (PFAG)

Peres full adder gate is a reversible full adder logic gate. It has 4 inputs, A, B and Cin with one of the inputs is '0'. Since it is a reversible logic circuit, it also produces 4 outputs, P, Q, Sum and Cout. The equations for the outputs are given by equations *Eq. 8*, *Eq. 9*, *Eq. 10* and *Eq. 11*.

$$P = A \quad \textit{Eq. 8}$$
$$Q = A \oplus B \quad \textit{Eq. 9}$$
$$Sum = A \oplus B \oplus C_{in} \quad \textit{Eq. 10}$$
$$C_{out} = (A \oplus B)C_{in} \oplus AB \quad \textit{Eq. 11}$$

By using the equations for the outputs, the hierarchical design method is used to design the Peres full adder gate in the CMOS technique. To design PFAG, two Peres gates are required as shown in Figure 5.

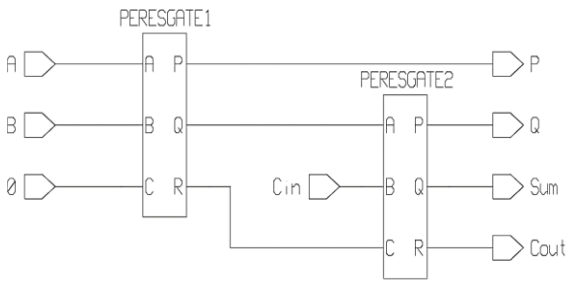

Figure 5: The schematic design for the Peres full adder gate

2.5 Design of 4-bit Multiplier

A 4-bit reversible multiplier is designed by using a combination of Peres gate and PFAG while a 4-bit conventional multiplier is designed by using a combination of half adder and full adder. The multiplier is based on Wallace tree architecture and needs two circuits to produce the outputs. Those two circuits are 4*4 reversible multiplier circuits ana reversible circuits for producing partial products.

Wallace tree technique [2] is a technique that executes the multiplication operation in parallel by producing three stages that consist of full-adder and half-adder circuits. The first stage is the respective multiplicand bit which is multiplied with each bit of the multiplier input and results in n^2 partial products. In the second stage, the partial product count is reduced with the use of full-adder and half-adder blocks. In the last stage, two n-sets results are added from the previous stage to an n-bit adder. If there are more than three bits with the same value, the second stage needs to add these by entering them into the full adder which produces one bit with equal value and another bit with a greater value. Two bits are put into a half adder if the same value remains. Transferral to the following layer will occur if only one bit is involved.

There are 16 partial products resulting from the product of two 4-bit digits x_n and y_n where n = 3, 2, 1, 0. In this project, the reversible Peres gate (for reversible multiplier) and half adder (for conventional multiplier) are used to compute the partial products. After that, the multiplier based on the Wallace technique is designed by using PFAG and Peres gate for reversible multiplier while full adder and half adder for a conventional multiplier. The circuits are shown in Figure 6 and Figure 7.

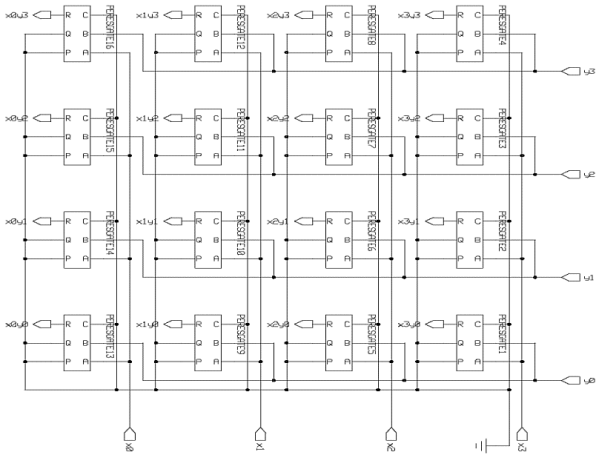

Figure 6: Circuit for producing products using Peres gate

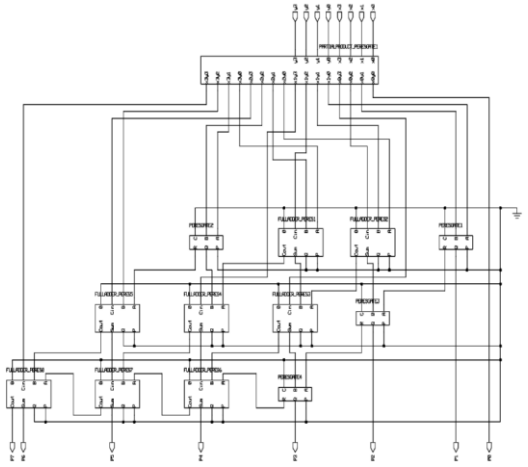

Figure 7: The 4-bit multiplier based on the Wallace technique

After the partial products are generated, all three partial products with the same value are classified and fed into full adders. One-half adder is used if two partial products with the same value remain. Furthermore, if there is just one partial product left, it will be transferred to the next layer. Finally, in the last stage, the result of two bits is added to a 4-bit carry ripple adder [2]. Based on the Wallace architecture, the multiplier required five full adders, three half adders, and one 4-bit adder. Since designing a 4-bit ripple carry adder needs one-half adder and 3 full adders, hence the total full adder needed is eight and four for half adders. In this project, the PFAG is used as a full adder and the Peres gate is used as a half adder by changing the input C into '0'.

3. Results and Discussion

3.1 Result of Half Adder. Full Adder, Peres gate and PFAG.

The resulting waveform for all four simulated gates in Figure 8, Figure 9, Figure 10 and Figure 11 are similar to the theoretical value. Thus, it can be concluded that the simulated gates are functioning according to the theory.

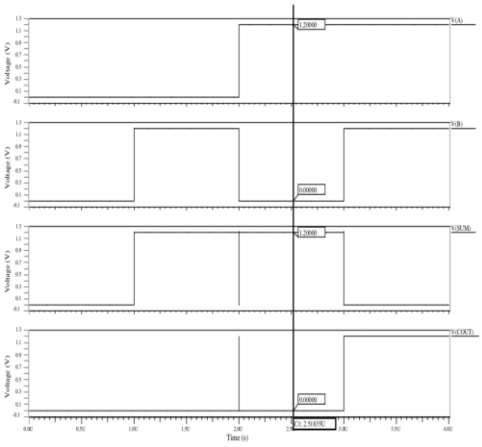

Figure 8: Waveform of half adder

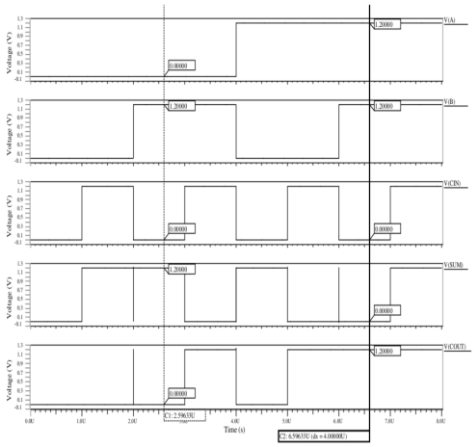

Figure 9: Waveform of Full adder

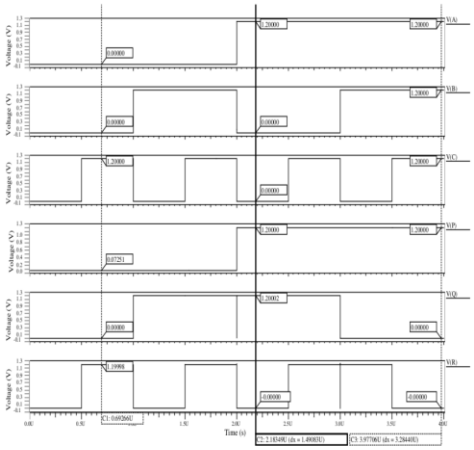

Figure 10: Waveform of Peres gate

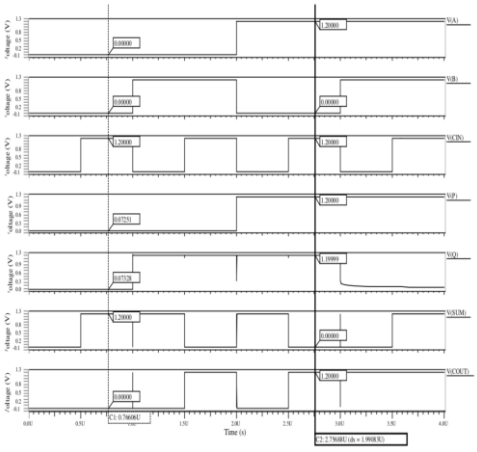

Figure 11: Waveform of Peres full adder gate

3.2 Result of 4-bit Reversible Multiplier

In Figure 12, the waveforms of Y_n and X_n, where n = 0, 1, 2 and 3 are inputs to the reversible multiplier to get the output of Pn, where n = 0, 1, 2, 3, 4, 5, 6 and 7. For example, at the period of 5 µs to 6 µs where the inputs of Y and X are 14 and 2 respectively, the result of the output P is 28. Another example is when the inputs of Y and X are 9 and 14 respectively at the period of 8 µs to 10 µs, the output P result is 126. This simulation result shows that the simulated 4-bit multiplier is functioning as it should be.

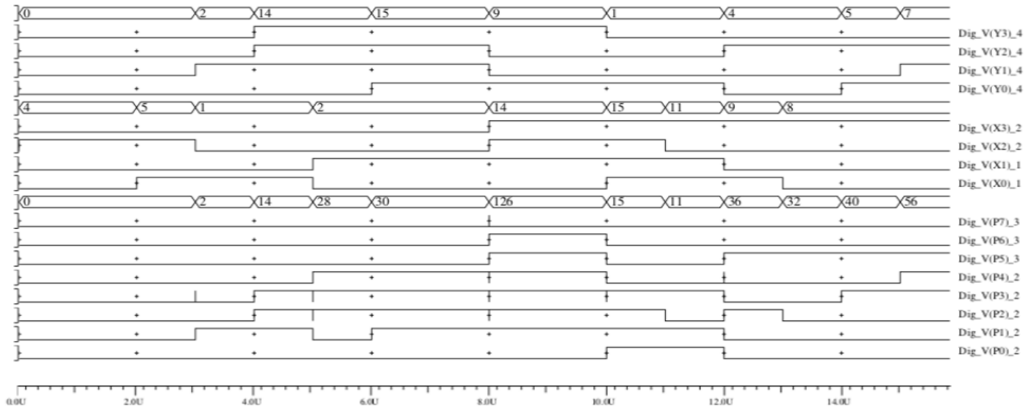

Figure 12: Waveform of 4-bit reversible multiplier

3.3 Power consumption of 4-bit Multiplier

The average power consumption was measured using a measurement tool for the conventional multiplier and reversible multiplier which is summarized in Table 1.

Table 1: The average power consumption by the multipliers

Average Power Consumption	1V	1.2V
130 nm Conventional Multiplier	714.94 µW	1.3050 mW
130 nm Reversible Multiplier	585.35 µW	1.0853 mW
180 nm Reversible Multiplier	975.57 µW	2.053 mW

Throughout 16 µs periods, the 130 nm reversible multiplier with 1V input voltage consumed 585.35 µW which is the lowest compared with the other simulated circuits. When the 130 nm reversible multiplier is compared with the 130 nm conventional multiplier, there is a slight difference in power consumed where the reversible multiplier used less power. Next is the comparison between 130 nm and 180 nm reversible multiplier. The result showed that the 130 nm reversible multiplier consumed less power twice as much which concluded that the lower CMOS technology used, the lower the power it consumed.

3.4 Delay Comparison for 4-bit Multiplier

The delays were measured as well using the measurement tool in Mentor Graphics software to determine the speed efficiency of both multipliers. Table 2 shows the delay for output "P0" for the conventional multiplier is 115.24 ps while for the reversible multiplier's delay is none. This is due to the value is too small for the tools to measure. This is also the same case for the output "P1", "P2", "P3" and "P6"

Table 2: The delay of each output for conventional and reversible multiplier

Delay Output	Conventional Multiplier	Reversible Multiplier
P0	115.24 ps	-
P1	165.99 ps	-
P2	206.41 ps	-
P3	205.35 ps	-
P4	219.74 ps	38.034 ps
P5	233.44 ps	58.462 ps
P6	171.48 ps	-
P7	703.95 ps	459.38 ps

(-) = The value too small to be measured

From Table 2, the results showed that the conventional multiplier's delays are much higher than the reversible multiplier's delays. From the results, the average delay is calculated for both conventional and reversible multipliers which are 252.7 ps and 69.48 ps respectively. Equation 12 is used to calculate the percentage delay.

$$\frac{Average\ dealay\ for\ reversible\ multiplier}{Average\ delay\ for\ conventional\ multiplier} \times 100\% = Speed\ percentage\ of\ multiplier \quad Eq.\ 12$$

From the calculated values, it can be concluded that the reversible multiplier is 27.5% faster than the conventional multiplier. This is because the reversible multiplier is using less gates as compared to the conventional multiplier.

4. Conclusion

In conclusion, the power consumption by the 130 nm reversible multiplier using 1 V is 585.35 µW while for the conventional multiplier is 714.94 µW. It is found that the power consumption for the reversible multiplier is lower compared to the conventional multiplier, and this proves that the objective of this project has been achieved. The objective also is accomplished where the delay is measured and compared between the conventional and reversible multiplier. From the results, the reversible multiplier is 27.5% faster than the conventional multiplier. The results also show that the designed multiplier is working according to the theory by providing the correct multiplier output. The results showed that all the objectives of the project have been achieved.

Acknowledgement

The authors would like to thank the Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia for its support.

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