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CMOS-based Instrumentation Amplifier for Biomedical Application

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Abstract: An instrumentation amplifier is normally used for the measurement of low-frequency signals including electrocardiogram (ECG), brain signals, nerve synapses pulses, etc. Biomedical signals usually are very weak due to low amplitude. An instrumentation amplifier which practically applied in biomedical applications is designed due to its numerous advantages such as gain can be adjusted easily by a single control without changing the whole structure and its common-mode rejection ratio (CMRR) is high. This project proposed a three op-amp instrumentation amplifier by using three two-stage complementary metal-oxide-semiconductor (CMOS) op-amp. This project is designed and simulated with Cadence Software using 130 nm CMOS technology. The gain of the proposed amplifier for pre-layout simulation is 64.15 dB with input-referred noise of 10.41 μ(V/√Hz) and power dissipation of 115.6 μW and a CMRR of 107.25 dB. The gain of the amplifier for post-layout simulation is 63.69 dB with input-referred noise of 10.52 μ(V/√Hz), the power dissipation of 115.6μ W, and CMRR of 100.39 dB. Apart from that, the amplifier is designed with a size layout of 5.25 x 10^4 μm^2.

Keywords: Biomedical Application, Instrumentation Amplifier, CMOS

1. Introduction

Nowadays, instrumentation amplifier is widely used in the medical field for instance used in medical application. An instrumentation amplifier is normally used for the measurement of low-frequency signals. Amplifier for ECG should have a gain of 1000 which is 60 dB and the common-mode rejection ratio (CMRR) should be above 100 dB [1]. Low-frequency signals including electrocardiogram (ECG), brain signals, nerve synapses pulses, etc. An amplifier that equips with the characteristic of high CMRR is suitable for biomedical detecting applications. So, low-frequency signals can amplify along with the rejection of noise. Instrumentation amplifiers can be used to suppress unwanted noise which will affect the original signal. An instrumentation amplifier is very crucial in a biomedical instrumentation system due to its high input impedance and high common-mode rejection ratio. Thus, unwanted signals can be rejected efficiently. Since the amplifier plays an important role in the whole system, some criteria are needed to have better performance. Normally, the signals are having a very low frequency and come along with the noise and thus the signals are disrupted. Once the

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frequency is low, the flicker noise of the transistor will be very high since the flicker noise is inversely proportional to the frequency of the input signal. Furthermore, it also should have criteria of high CMRR.

Figure 1 shows the schematic diagram of the instrumentation amplifier and Figure 2 shows the biomedical electronics detecting system blocks which including an electrode, amplifier, low pass filter, sample and hold circuit as well as analog to digital converter. The biomedical signal is detected and the useless interferences may also pick up by the electrode together. Biomedical electronics are unable to detect low amplitude signals. Therefore, application with good performance which consists of high gain, low input-referred noise, low power dissipation is required

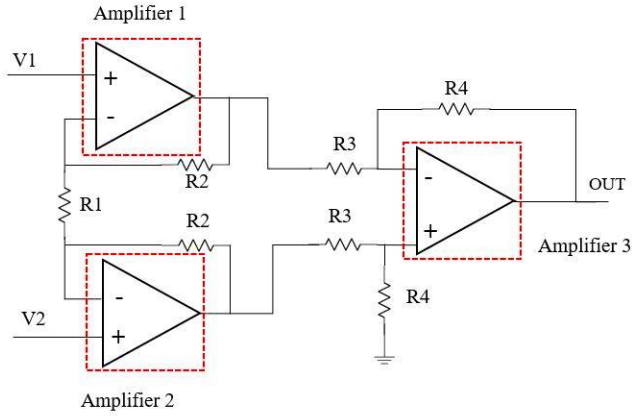


Figure 1: Schematic diagram of instrumentation amplifier

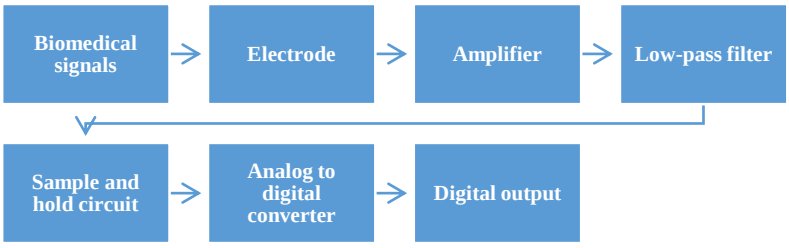


Figure 2: Biomedical electronics detecting system blocks

2. Methodology

The simulation of CMOS instrumentation amplifier for biomedical application is done using Cadence Software. High noise immunity and low static power consumption can be the most important characteristics of CMOS [2] since the transistor of the metal–oxide–semiconductor field-effect transistor (MOSFET) pair are off while the other one is on [3]. The amplifier is designed using 130 nm technology with a voltage supply of 1.2 V. Gain and CMRR of the designed amplifier should be above 60 dB and 100 dB respectively [1]. Power dissipation and input-referred noise of the designed amplifier should reach below 388 µW [4] and below 22.8 m(V/√Hz) [5] respectively as a reference value for the project to make an improvement.

Figure 3 shows the schematic of the two-stage CMOS op-amp. After that, the designed circuit will then be encapsulated into an op-amp circuit as shown in Figure 4 which is the schematic diagram of the proposed amplifier with the instrumentation amplifier connection as per figure 1 to do the simulation process and study as well as investigate the performance of the designed circuit which are differential gain, power dissipation, input-referred noise, and CMRR.

The instrumentation amplifier is designed using the Miller-Compensation Technique. A capacitor is connected between the first stage and second stage of the circuit. The compensation capacitor is used to improve the frequency response as well as to decrease the slew rate. of the amplifier. The compensation technique can help to reduce the power consumption of the whole circuit as well as to suppress unwanted noise. In order to prevent the amplifier become unstable and the occurrence of under-damped oscillatory time response, a two-stage op-amp is used and designed with a frequency compensation technique [3]. The most important characteristic of using this technique is to ensure the circuit remains stable [6].

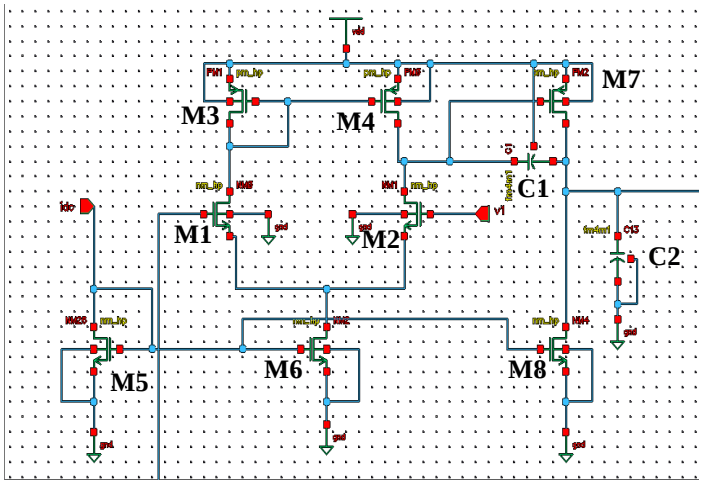


Figure 3: Schematic of two-stage CMOS op-amp

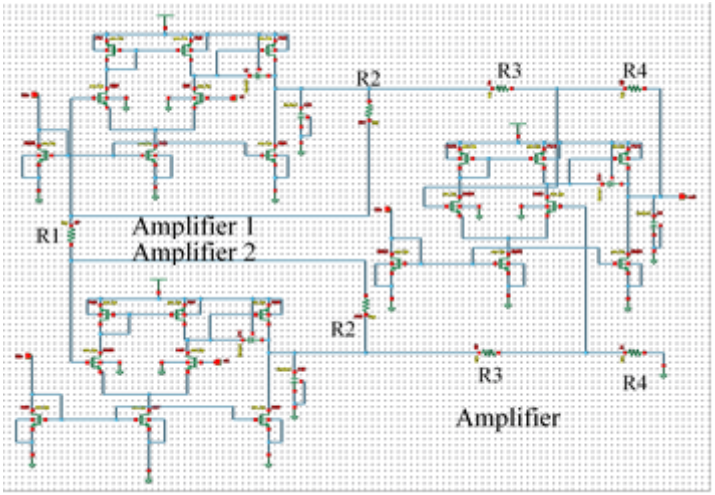


Figure 4: Schematic diagram of proposed amplifier

B_{eff} is defined as the current in over current out of the transistors in DC. To obtain parameters of $\mu_n C_{ox}$ and $\mu_p C_{ox}$, B_{eff} is obtained through the simulation. B_{eff} for NMOS is 4.34 $x10^{-3}$ which is approximately 4.50 $x10^{-3}$ and B_{eff} for PMOS is 1.20 $x10^{-3}$ which approximately 1.50 $x10^{-3}$ is obtained through the simulation. From Eq.1, the $\mu_n C_{ox}$ obtained is 450 $\mu A/V^2$, where (W/L) is 10 and B_{eff} is 4.50 $x10^{-3}$. From eq.2, the $\mu_p C_{ox}$ obtained is 150 $\mu A/V^2$, where (W/L) is 10 and B_{eff} is 1.50 $x10^{-3}$. B_{eff} stands for the beta effective, μ_n and μ_p represent the mobility of electron and proton respectively, C_{ox} is the capacitance oxide while the (W/L) is the ratio of width to length of transistors.

$$\mu_n C_{ox} \left(\frac{W}{L}\right) = B_{eff} \qquad Eq.1$$

$$\mu_p C_{ox} \left(\frac{W}{L}\right) = B_{eff} \quad Eq.2$$

Some specifications are fixed for calculation and simulation processes that aim to get the width of the transistors as shown in Table 1. The threshold voltage of PMOS and NMOS is obtained through the simulation process to obtain the width and length of the transistors as shown in Table 2.

Table 1: Specifications for calculation purpose

Gain bandwidth, GBW	30 MHz
Slew rate, SR	20 V/µsec
Input common-mode range (max), $ICMR_{max}$	1.0 V
Input common-mode range (min), $ICMR_{min}$	0.5 V
Load capacitor, C_L	2 pf
Voltage supply, V_{dd}	1.2 V

Table 2: Threshold voltage for PMOS and NMOS

	when ICMR (max) is applied (1 V)	When ICMR (min) is applied (0.5 V)
Threshold voltage of PMOS, Vtp (V)	-319m	-319m
Threshold voltage of NMOS, Vtn (V)	364.7m	279.6m

The capacitance of the compensation capacitor is obtained by using eq.3 and the compensation capacitor's capacitance obtained is 800 fF. C_L represents the load capacitor which is fixed in Table 1. Next, current flow through the transistor M5 is obtained by using Eq.4. From Eq.4, current flow through transistor M5, I_5 is 16 µA which approximates 20 µA where slew rate, SR is 20 V/µsec.

$$Compensation\ capacitor, C_C = 0.22C_L \quad Eq.3$$

$$Slew\ rate, SR, = \frac{I5}{C_C} \quad Eq.4$$

Before obtaining the ratio of width to length of M1 and M2, the transconductance of M1 is obtained by using Eq.5 with the value of 160 µS. GBW represents the gain bandwidth fixed in table 1 and C_c represents the capacitance of the compensation capacitor. After the transconductance of M1 is obtained, the ratio of width over the length of M1 and M2 is obtained through eq.6 with a value of 2.84 which is approximate 3. The current flow through M1, I_{d1} is 10 µA.

$$Transconductance\ of\ M1, g_{m1} = GBW\ x\ Cc\ x\ 2\pi \quad Eq.5$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m1})^2}{(\mu_n C_{ox})(2I_{d1})} \quad Eq.6$$

From Eq.7, the ratio of width to length of M3 and M4 obtained is 5.21 which is approximate 6. V_{dd} represents the voltage supplied to the amplifier, $ICMR_{(max)}$ represents the maximum input common-mode range which is fixed in Table 1, I_{d3} is the current flow through M3. $V_{t3(max)}$ and $V_{t1(min)}$ stand for the maximum and minimum threshold voltage for M3 and M1.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2I_{d3}}{(\mu_P C_{OX})(V_{dd} - ICMR_{max} - V_{t3(max)} + V_{t1(min)})^2} \quad Eq.7$$

The saturation voltage of transistor M5 is computed from eq.8 with the value of 0.018 V. However, if saturation voltage was below 100 mA, the transistor will operate at the triode region. Adjustment of the ratio of width to the length of transistors M1 and M2 is made. The ratio is changed to 28 and the saturation voltage obtained is 0.1002 V. $ICMR_{(min)}$ represents the minimum input common-mode range. After the important parameters are obtained, the ratio of width to length of transistor M5 and transistor M6 is computed from Eq.9 which is 8.85 and approximate to 9.

$$Saturation\ voltage, V_{DSAT} = ICMR(min) - \sqrt{\frac{2I_{d1}}{\mu_n C_{ox}(W/L)_{1,2}}} - V_{t1max} \quad Eq.8$$

$$(\frac{W}{L})_{5,6} = \frac{2I_{d5}}{(\mu_n C_{ox})(V_{DSAT})^2} \quad Eq.9$$

Before obtaining the ratio of width to length of transistors M7, the transconductance of transistors M4 and M7 is obtained by using Eq.10 and 11 respectively with the value of 134 µS and 1600 µS. From Eq.12, the ratio of width over the length of transistors 7 is computed which is 71.64 and approximate to 72.

$$Transconductance, g_{m4} = \sqrt{(\mu_p C_{ox})\ x\ (\frac{W}{L})_{3,4}\ x\ 2I_{d4}} \quad Eq.10$$

$$Transconductance, g_{m7} = 10 g_{m1} \quad Eq.11$$

$$(\frac{W}{L})_7 = \frac{g_{m7}}{g_{m4}} x (\frac{W}{L})_4 \quad Eq.12$$

Current flow through the transistor M7 is computed from Eq.13 which is 120 µA. Based on Eq.14, the transistors width to length ratio is computed with (W/L) of 54.

$$I_7 = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_4} x\ I_4 \quad Eq.13$$

$$(\frac{W}{L})_8 = \frac{I_7}{I_5} x (\frac{W}{L})_5 \quad Eq.14$$

Table 3 shows the width and length of the transistors for the designed amplifier, the length of all the transistors fixed at 500 nm. The ratio of width to length of transistor M1 and M2 is 28, M3 and M4 are 6, M5 and M6 is 9 M7 and M8 is 72 and 54 respectively. Table 4 displays the resistance for each of the resistors used for the designed amplifier to meet the requirement as predetermined.

Table 3: Width and length of the transistor

Transistor	Width and length
M1, M2	L=500 nm W=14 µm
M3, M4	L=500 nm W=3 µm
M5, M6	L=500 nm W=4.5 µm
M7	L=500 nm W=36 µm
M8	L=500 nm W=27 µm

Table 4: Proposed resistor value

Resistor	Resistance (kΩ)
R1	3
R2	100
R3	3
R4	100

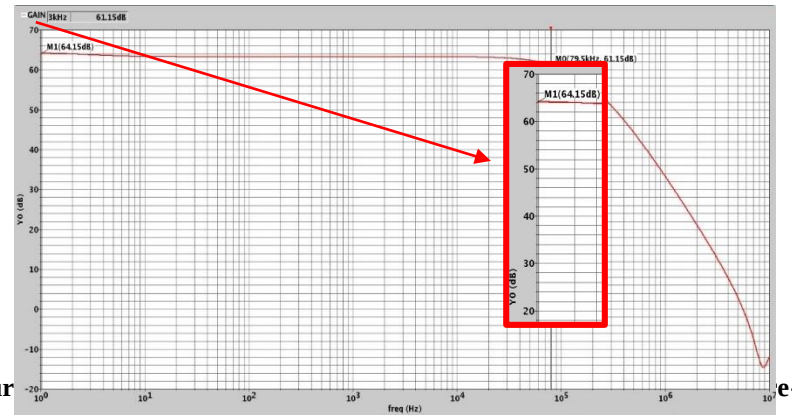
3. Results and Discussion

Figure 5 shows the differential gain of the proposed instrumentation amplifier during pre-layout simulation. The theoretical gain calculates using Eq.15 obtained is 67.07 dB. After the pre-layout simulation is carried out, the differential gain of the proposed instrumentation amplifier is 64.15 dB. Cut off frequency of the designed amplifier is 75.9 kHz.

Theoretical calculation;

$$Differential\ gain, A_D = (\frac{R4}{R3})(1 + \frac{2R2}{R1}) \qquad Eq.15$$

$$20\ log\ (1 + \frac{2\ (100\ K)}{3\ K})(\frac{100\ K}{3\ K})) = 67.07\ \text{dB} \qquad Eq.16$$



Figur e-layout)

Total power dissipation comprises static power dissipation as well as dynamic power dissipation. Static power dissipation will be occurred because of the leakage of current while the occurrence of dynamic power dissipation is due to the charging and discharging of the transistor dissipation. When the static power dissipation and the dynamic power dissipation of transistors are decreased, the total power dissipation for the whole circuit also will be reduced. This can be made by lower the power supply for the whole circuit. It is because static power dissipation is directly proportional to the power supply as stated in Eq.17. The power dissipation of the proposed instrumentation amplifier measured is 115.6 µW as shown in Figure 6.

$$P_{static} = V_{dd}\ x\ I \qquad Eq.17$$

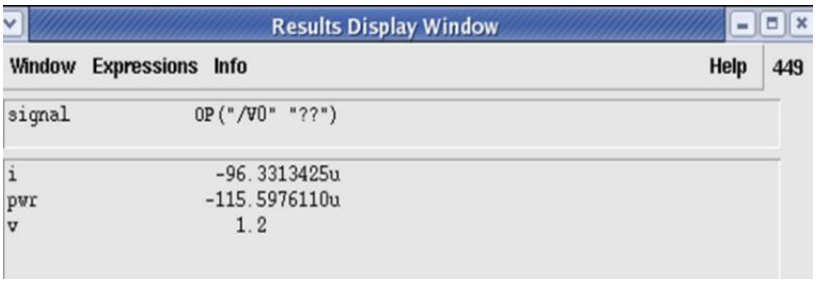


Figure 6: Power dissipation of instrumentation amplifier (Pre-layout)

Input referred noise is the combination of flicker noise as well as thermal noise. But will more concentrate on the flicker noise since noise in the surrounding will affect the biomedical signal because the signal is very low frequency and low amplitude. Flicker noise is varied accordingly by the changes of width and length of the transistor [7] as stated in Eq.18. From the simulation result, the input-referred noise of the instrumentation amplifier measured is 10.41 μ(V/√Hz) as shown in Figure 7. K is the transistor flicker noise factor, f stands for the frequency of the signal, (W/L) represents the ratio of width to length of the transistors and C_{ox} stands for the gate capacitance per unit area.

$$Flicker\ noise, \overline{V_n^2} = \frac{K}{f(W/L)C_{OX}} \qquad Eq.18$$

Figure 7: Input referred noise of instrumentation amplifier (Pre-layout)

The common-mode gain measured is -43.1 dB as shown in Figure 8. There is a "bum" shape occurred at around frequency of 10^5 Hz due to the occurrence of fluctuation. The differential gain measured is 64.15 dB as shown in Figure 5. So, the CMRR of the proposed instrumentation amplifier measured is 107.25 dB by calculating using Eq.19. A_D represents the differential gain of the amplifier while A_C represents the common-mode gain of the amplifier.

$$CMRR = 20log(\frac{A_D}{A_C}) \qquad Eq.19$$

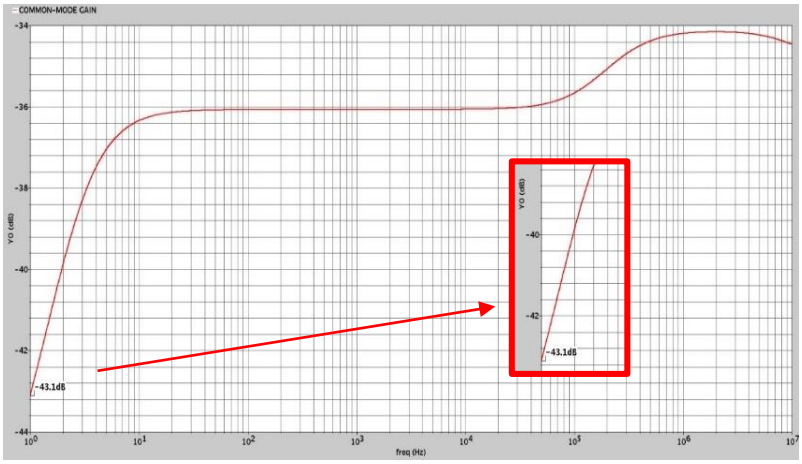


Figure 8: Common mode gain of the instrumentation amplifier (Pre-layout)

Figure 9 shows the layout of the proposed instrumentation amplifier for biomedical applications. Post-layout simulation is carried out right after the calibre of design rule check (DRC), layout versus schematic (LVS), and parasitic extraction (PEX) with no occurrence of any errors. Through the post-layout simulation, all the design constraints will be verified. Post-layout simulation is considered an important step before it prepares for the fabrication process. During post-layout simulation, a more precise analog model design can be created with the extracted parasitic capacitance and resistance. Method of design the layout such as width or length of the transistors, finger of transistors, etc will affect the performance of the designed circuit. The width and length of the transistor will affect the current flow. Once the current flow is low, the performance of the circuit will degrade. Thus, there will occur a slight difference between the pre-layout simulation and the post-layout simulation results.

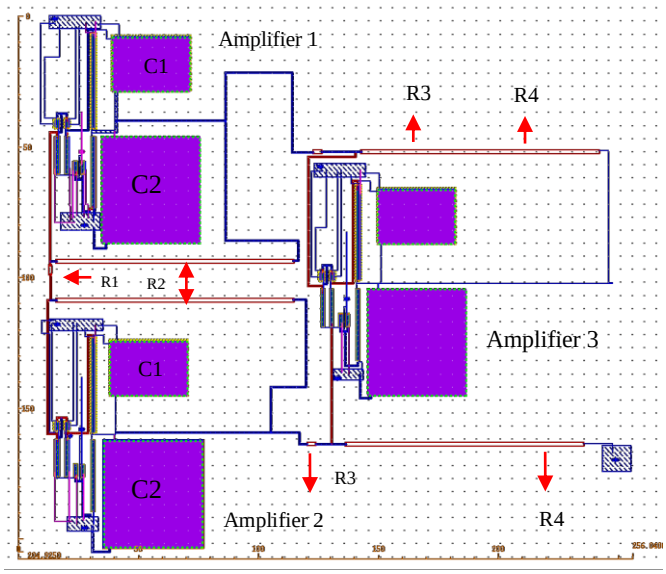


Figure 9: Layout of proposed amplifier

The differential gain of the proposed instrumentation amplifier obtained in post-layout simulation is 63.69 dB as shown in Figure 10. Cut off frequency obtained in pre-layout simulation is 79.5 kHz and 162.5 kHz in post-layout simulation. The input-referred noise of the designed instrumentation amplifier acquired from the post-layout simulation is 10.52 μ(V/√Hz) as shown in Figure 11. The common-mode gain of the proposed instrumentation amplifier is measured from the

post-layout simulation is -36.7 dB as illustrated in Figure 12. Figure 13 displays the power dissipation of the proposed instrumentation amplifier obtained from post-layout simulation which is 115.57 µW.

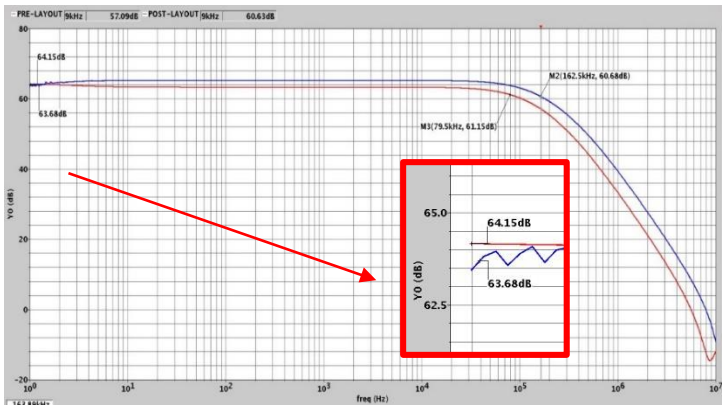


Figure 10: Differential gain of the instrumentation amplifier (Pre-layout & Post-layout)

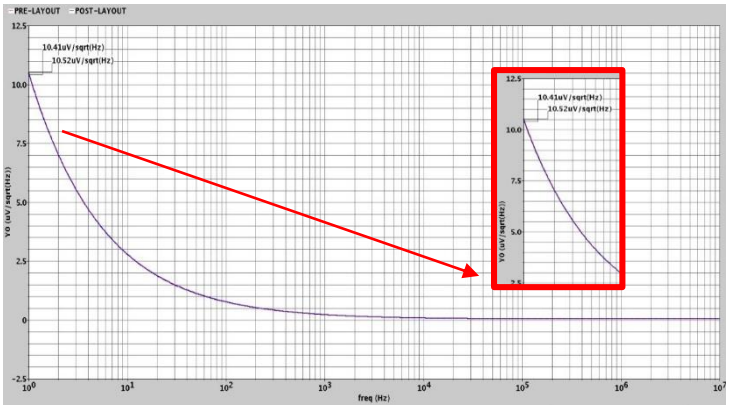


Figure 11: Input referred noise of instrumentation amplifier. (Pre-layout & Post-layout)

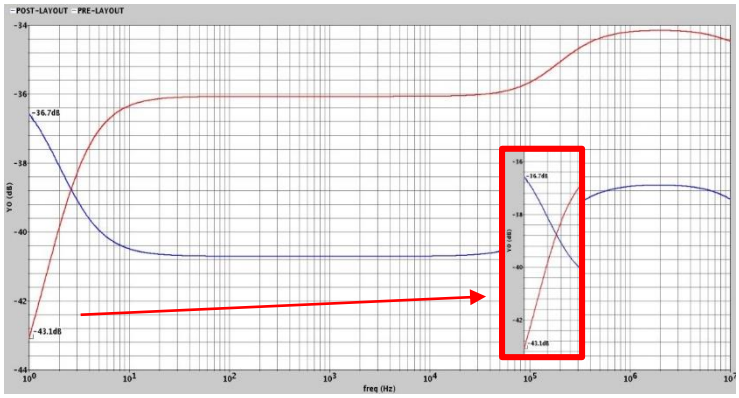


Figure 12: Common mode gain of the instrumentation amplifier (Pre-layout & Post-layout)

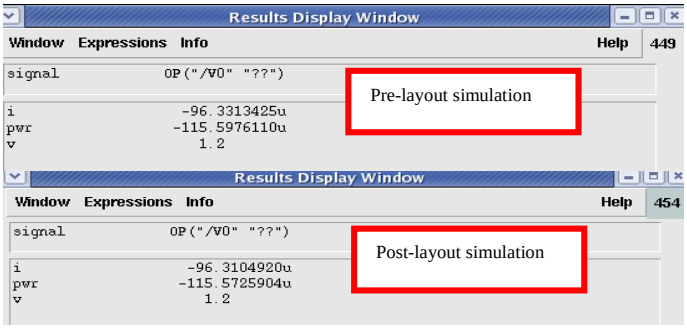


Figure 13: Power dissipation of instrumentation amplifier (Pre-layout & Post-layout)

Table 5 shows a comparison between the proposed value, pre-layout as well as post-layout simulation value. The value of pre-layout simulation and post-layout simulation has a small difference but it is still acceptable. The small difference is due to the technique used to create the layout by varying the number of fingers of the components which can affect the performance of the whole circuit and the width or length of the transistor also may affect the result. The width and length of the transistor will affect the current flow. Once the current flow is low, the performance of the circuit will degrade. Apart from that, post-layout simulation has included the parasitic capacitances which can provide a more precise analog model. However, the parasitic capacitances affect the performance of the proposed instrumentation amplifier.

Table 5: Comparison between proposed value, pre-layout and post-layout simulation value

	Proposed value	Pre-layout simulation	Post-layout simulation
Technology used (nm)		130	
Voltage supply (V)		1.2	
Gain (dB)	Above 60	64.15	63.69
Power dissipation (W)	Below 388µ	115.6µ	115.6µ
Input referred noise (V/√Hz)	Below 22.8m	10.41µ	10.52µ
CMRR (dB)	Above 100	107.25	100.39

4. Conclusion

In a conclusion, the proposed 130nm CMOS-based instrumentation amplifier is constructed successfully using Cadence Software and the simulation results also achieved the desired value. The gain of the designed amplifier for pre-layout simulation achieved is 64.15 dB with input-referred noise of 10.41 µ(V/√Hz) and power dissipation of 115.6 µW as well as the CMRR of the amplifier designed is 107.25 dB. Apart from that, the gain of the amplifier for post-layout simulation achieved is 63.69 dB with input-referred noise of 10.52 µ(V/√Hz), the power dissipation of 115.6 µW and CMRR of 100.39 dB. Apart from that, the amplifier is designed with a size layout of 5.25x104 μm^2.

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