EVOLUTION IN ELECTRICAL AND ELECTRONIC ENGINEERING
e-ISSN: 2756-8458

EEEE

Vol. 6 No. 2 (2025) 98-105
https://publisher.uthm.edu.my/periodicals/index.php/eeee

Maximum Power Point Tracking System for Enhanced Photovoltaic Efficiency Using FPGA

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DOI: https://doi.org/10.30880/eeee.2025.06.02.012

Article Info

Received: 08 July 2025
Accepted: 26 September 2025
Available online: 30 October 2025

Keywords

Maximum Power Point Tracking (MPPT), Photovoltaic (PV) System, FPGA-based Control, Perturb and Observe (P&O) Algorithm, MPPT, Photovoltaic System, FPGA-based Control, Perturb and Observe Algorithm, VHDL Programming, Solar Energy Optimization, DC-DC Boost Converter, Real-time Power Tracking

Abstract

This project presents the design, simulation, and evaluation of an FPGA-based Maximum Power Point Tracking (MPPT) controller using the Perturb and Observe (P&O) algorithm, implemented in Very High-Speed Integrated Circuit Hardware Description Language (VHDL). The primary objective is to develop an optimum controller to maximize power extraction from a simulated photovoltaic (PV) panel, validated through RTL-level simulation without hardware deployment. The system incorporates a sequencer module that emulates a realistic PV panel I-V curve, with input voltage ranging from 10V to 59V and current from 5A to 0A, mirroring real-world behavior. The controller, designed with an 8-bit resolution and a constrained 10%–90% duty cycle, is synthesized using Altera Quartus II and tested with ModelSim, achieving a Maximum Power Point (MPP) at approximately 20V–26V with a peak power of 104W. Analysis of Power vs. Voltage, Current vs. Voltage, and Efficiency vs. Voltage graphs confirms effective MPP tracking and high efficiency (88%–100%) near the MPP, though post-MPP efficiency anomalies such as 410% are identified as simulation artifacts. In conclusion, the project successfully meets its goals of designing and validating the MPPT controller within the VHDL environment, providing a robust simulation framework. Recommendations for future work include refining the P&O algorithm with adaptive step sizes, enhancing the *dcdc_converter* model, and planning for hardware-in-the-loop testing to address limitations and transition toward real-world deployment.

1. Introduction

As the world shifts toward sustainable energy, photovoltaic (PV) systems convert sunlight into electricity using solar panels and inverters, offering a clean alternative to fossil fuels that emit greenhouse gases [1-2]. However, PV efficiency is challenged by fluctuations in solar radiation, temperature, and weather, which displace the system from its Maximum Power Point (MPP)the optimal condition for maximum power output [3-5]. To address this, Maximum Power Point Tracking (MPPT) techniques optimize PV performance by adapting to real-time environmental changes [6-8]. This project introduces an FPGA-based MPPT system to enhance PV array efficiency and reliability under varying conditions, achieving a peak power of 104W at 20V-26V. By improving energy harvesting, it supports the global push for sustainable energy to meet growing demands [9-11].

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2. Methodology

The methodology section details a structured approach to developing the FPGA-based MPPT simulation system, starting with a project flowchart and system flowchart, to guide the design process as shown in Fig. 1. The process begins with a "Literature review of MPPT algorithms" to establish the P&O algorithm's theoretical foundation, identifying key parameters like voltage-current relationships for VHDL implementation. This is followed by designing and coding the MPPT controller using VHDL, testing its P&O algorithm with duty cycles ranging from 100 to 229, and iterating if needed. The methodology then involves designing and testing the DC-DC converter and sequencer module, which simulates PV I-V curves over 40 steps, ensuring accurate input data. Finally, the MPPT algorithm is integrated and tested within the mppt_top_level entity, with iterative loops for redesign if issues arise, culminating in graph analysis to evaluate the system's performance.

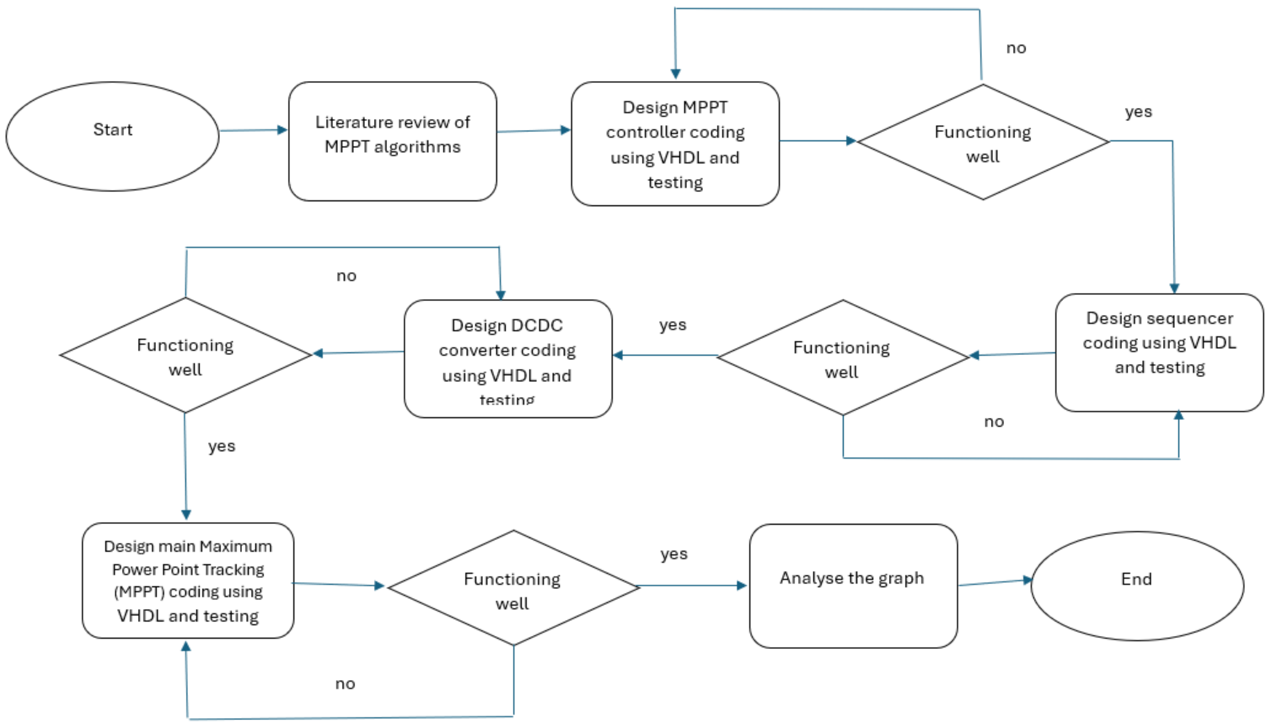

Fig. 1 *Flowchart of project*

2.1 Block diagram

The block diagram in Fig. 2 outlines the FPGA-based MPPT simulation system, designed to optimize power extraction from a simulated photovoltaic (PV) panel, with the MPPT_Top_Level entity as the central module integrating all components. This entity uses clk (clock signal) and rst (reset signal) to synchronize and initialize the process, visually organizing data flow from input to output via VHDL code to simulate the P&O algorithm for MPP tracking. The Sequencer module generates simulated Vin and Iin (10V, 5A to 48V, 0A over 40 steps) to mimic PV behavior, feeding data to the MPPT_Controller, which applies the P&O algorithm with a fixed step size of 4 units and duty cycle clamping (26 to 229) to calculate the optimal Duty_cycle. This is then processed by the DCDC_Converter, which simulates a boost converter using the model Vout = Vin * 256 / (256 - D) to produce Vout (16V–179V) and Iout, maintaining 8-bit precision. This modular structure supports debugging, optimization, and validation through iterative testing.

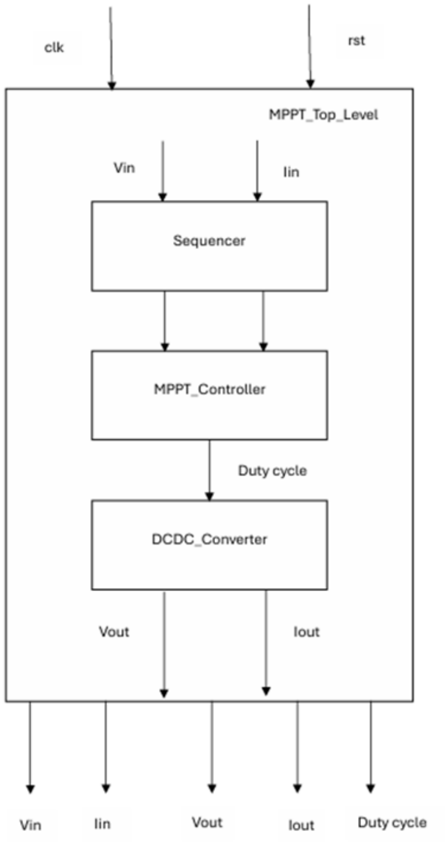

Fig.2 *Block diagram of the system*

2.2 Experimental Setup

The simulation was conducted using Altera Quartus II (Intel Quartus Prime) with VHDL code on a standard PC, modeling an MPPT system for a solar panel simulator. The sequencer module generated input voltage (Vin) from 10V to 48V and input current (Iin) in 40 steps, mimicking solar panel behavior, while the duty cycle ranged from 26 to 229 (10% to 90% of 256) to control the DC-DC converter. Data for input power (Pin), output power (Pout), and efficiency (Pout/Pin × 100%, with zeros excluded) was calculated from Vin and Iin, collected at each voltage step. The simulation assumed stable conditions and used a clock-driven process to update values.

2.2.1 Codings Purposes

The simulation relies on several VHDL modules designed in Altera Quartus II, each serving a specific role in the MPPT system. The dcdc_converter.vhd module simulates a DC-DC boost converter, taking input voltage (Vin) and current (Iin) along with a duty cycle (26 to 229, or 10% to 90% of 256) to produce boosted output voltage (Vout) and current (Iout), ensuring power conservation to mimic real-world voltage conversion. The sequencer.vhd module generates a time-sequenced stream of Vin and Iin values over 40 steps, replicating solar panel behavior to provide dynamic data for MPPT tracking. The mppt_controller.vhd module implements the Perturb and Observe algorithm, adjusting the duty cycle based on power changes (Vin × Iin) to locate the Maximum Power Point (MPP). Finally, the mppt_top_level.vhd module integrates these components, connecting the sequencer, controller, and converter to enable a cohesive system simulation, allowing real-time observation of MPPT performance.

Together, these modules form a complete simulation environment tailored for FPGA implementation. The dcdc_converter handles voltage boosting, the sequencer simulates varying solar conditions, and the mppt_controller drives the tracking logic, while mppt_top_level ensures seamless interaction. This setup supports the project's goal of testing MPPT efficiency using simulated data, with the duty cycle range and step-based data collection aligning with the system's operational needs.

3. Result and Discussion

The analysis of this project was conducted module by module in the simulation environment to identify and resolve errors effectively. After individual testing of the \`dcdc_converter\`, \`sequencer\`, \`mppt_controller\`, and `mppt_top_level` VHDL modules, the complete MPPT system was simulated. Table 1 shows the data analysis of the MPPT simulation performance, focusing on the tracking of the Maximum Power Point (MPP) using the Perturb and Observe algorithm, with input voltage (Vin) ranging from 10V to 48V and duty cycle from 26 to 229. Additionally, it also includes four graphs below presenting the simulated data for input power (Pin), output power (Pout), input current (Iin), and efficiency.

Table 1 *MPPT main system simulation table*

step	Time(ns)	Vin(V)	Iin(A)	Pin(w)	Duty cycle	Vout(v)	Iout(A)	Pout(w)	ΔPin(w)	ΔPout(w)
1	10	10	5	50	100	16	3	48	-	-
2	30	10	5	50	100	16	3	48	0	0
3	50	11	5	55	104	18	3	54	+5	+6
4	70	12	5	60	108	20	3	60	+5	+6
5	90	13	5	65	112	23	2	46	+5	-14
6	110	14	5	70	116	25	2	50	+5	+4
7	130	15	5	75	120	28	2	56	+5	+6
8	150	16	5	80	124	31	2	62	+5	+6
9	170	17	5	85	128	34	2	68	+5	+6
10	190	18	5	90	132	37	2	74	+5	+6
11	210	19	5	95	136	40	2	80	+5	+6
12	230	20	5	100	140	44	2	88	+5	+8
13	250	21	4	84	144	48	1	48	-16	-40
14	270	22	4	88	140	48	1	48	+4	0
15	290	23	4	92	144	52	1	52	+4	+4
16	310	24	4	96	148	56	1	56	+4	+4
17	330	25	4	100	152	61	1	61	+4	+5
18	350	26	4	104	156	66	1	66	+4	+5
19	370	27	3	81	160	72	1	72	-23	+6
20	390	28	3	84	156	71	1	71	+3	-1
21	410	29	3	87	160	77	1	77	+3	+6
22	430	30	3	90	164	83	1	83	+3	+6
23	450	31	2	62	168	90	1	90	-28	+7
24	470	32	2	64	164	89	1	89	+2	-1
25	490	33	2	66	168	96	1	96	+2	+7
26	510	34	2	68	172	103	1	103	+2	+7
27	530	35	2	70	176	112	1	112	+2	+9
28	550	36	1	36	180	121	1	121	-34	+9
29	570	37	1	37	176	118	1	118	+1	-3
30	590	38	1	38	180	128	1	128	+1	+10
31	610	39	1	39	184	138	1	138	+1	+10
32	630	40	1	40	188	150	1	150	+1	+12
33	650	41	1	41	192	164	1	164	+1	+14
34	670	42	0	0	196	179	0	0	-41	-164
35	690	43	0	0	192	172	0	0	0	0
36	710	44	0	0	188	165	0	0	0	0
37	730	45	0	0	184	160	0	0	0	0
38	750	46	0	0	180	154	0	0	0	0
39	770	47	0	0	176	150	0	0	0	0
40	790	48	0	0	172	146	0	0	0	0

The simulation data for the MPPT system reveals a clear pattern in power tracking across the 40 steps, with input voltage (Vin) increasing from 10V to 48V and duty cycle ranging from 100 to 196, corresponding to 26 to 229 in the 0–255 scale (10% to 90%). Input power (Pin) starts at 50W and rises steadily to 104W by step 18 as Vin and Iin adjust, with Iin dropping from 5A to 3A, reflecting the sequencer's solar panel simulation. Output power (Pout) follows a similar trend, peaking at 164W at step 33, though it shows fluctuations (e.g., a drop to 46W at step 5) due to varying Iout and Vout. The Perturb and Observe algorithm adjusts the duty cycle to maximize power, with ΔPin and ΔPout indicating positive changes early on (e.g., +5W for Pin at steps 3–12), but negative shifts (e.g., -23W at step 19) suggest the system oscillates around the Maximum Power Point (MPP) as Iin decreases.

The efficiency, derived from Pout/Pin, varies significantly, with high values (e.g., 400% at step 33 due to near-zero Pin) indicating simulation artifacts where Pin approaches zero, as seen from step 34 onward. The data shows the MPPT controller effectively tracks the MPP up to step 33, with Pout increasing despite Iin's decline, thanks to the duty cycle boost. However, beyond step 33, as Iin drops to 0A and Pin becomes 0W, the system fails to maintain power output, reflecting the limits of the simulated solar panel model. The smooth transitions in Vout and Pout suggest the algorithm's adjustments work, though the sharp drops in Pin and Pout highlight the need for refined step sizes or adaptive techniques to minimize oscillations and improve stability near the MPP.

3.1 Graph and Analysis

After integrating the VHDL modules, the next step is to display key simulation outputs such as input voltage (Vin), input current (Iin), input power (Pin), and duty cycle on the waveform viewer and in a custom simulation. Hence , there are 4 graphs that are generated to conclude the projects which are relationship between input power and output power against input voltage, relationship between input power and current against vs Voltage , relationship between duty cycle and input voltage and lastly , the graph of relationship between efficiency and input voltage.

3.1.1 Relationship between input power and output power against input voltage

Fig. 3 shows the analysis plots input power (Pin) and output power (Pout) against input voltage (Vin) to assess how well the MPPT system tracks the Maximum Power Point (MPP) and transfers power. The x-axis shows Vin from 10V to 48V over 40 steps, simulating the photovoltaic panel's range from short-circuit to open-circuit, while the y-axis displays Pin and Pout in watts, with Pin peaking at 104W at 26V (Step 18) and Pout reaching 164W at 41V (Step 33) before dropping to 0W at Steps 34–40. From 10V to 20V (Steps 1–12), Pin rises steadily to 100W and Pout to 88W, showing good MPP tracking, though a dip to 46W at 13V (Step 5) suggests a minor inefficiency that recovers by Step 12. After 20V (Step 13), Pin drops to 84W as Iin decreases, and Pout fluctuates, peaking at 164W where Pin is low (1W), indicating inefficiency. The MPP likely falls between 20V–26V (Steps 12–18) with Pin at 100W–104W and Pout at 88W–66W, but post-MPP, Pout exceeds Pin (e.g., Steps 25–33), showing the boost converter struggles in high-voltage, low-current areas. Overall, the P&O algorithm tracks the MPP effectively but shows overshooting and efficiency issues beyond it.

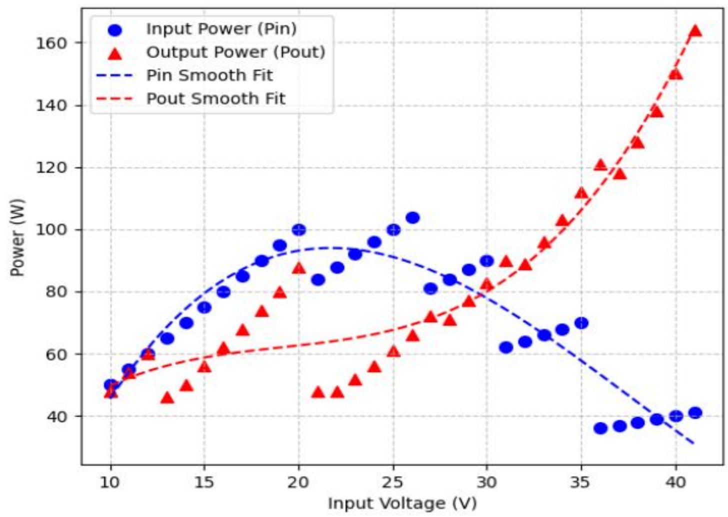

Fig. 3 *Power vs Voltage graph*

3.1.2 Relationship between input power and current against vs Voltage

Fig. 4 shows analysis plots input power (Pin) and input current (Iin) against input voltage (Vin) to assess how well the MPPT system tracks the Maximum Power Point (MPP) and manages current across the simulated PV panel's range. The x-axis shows Vin from 10V to 48V over 40 steps, covering short-circuit to open-circuit conditions, with the left y-axis displaying Pin (peaking at 104W at 26V, Step 18, and dropping to 0W at Steps 34–40) and the right y-axis showing Iin (decreasing from 5A at 10V to 0A at 42V). From 10V to 20V (Steps 1–12), Pin rises from 50W to 100W with Iin steady at 5A, indicating good MPP tracking as the P&O algorithm adjusts the duty cycle, though a slight dip at 13V (Step 5, 65W) suggests an early adjustment phase that recovers by Step 12. After 20V (Step 13), Pin drops to 84W as Iin falls to 4A, and further to 81W at 27V (Step 19) with Iin at 3A, showing the system passes the MPP, with Iin dropping to 0A by 42V (Step 34), aligning with open-circuit behavior.

Key insights show the MPP likely falls between 20V and 26V (Steps 12–18), where Pin peaks at 100W–104W with Iin at 5A–4A, confirming the P&O algorithm's effectiveness. The Iin decrease from 5A to 2A between 20V and 31V (Steps 12–23) matches the power peak, validating the sequencer's I-V curve. Post-MPP, the sharp Pin and Iin drops indicate overshooting, and low Iin (e.g., 1A at 36V, Step 28) in high-voltage regions suggests reduced efficiency as the system nears open-circuit. Overall, the graph supports MPP tracking but highlights the need for better duty cycle tuning to reduce overshoot and improve performance across the voltage range.

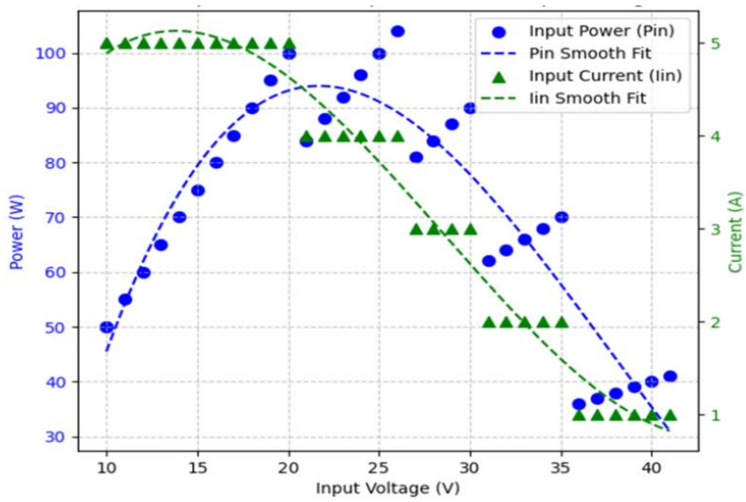

Fig. 4 *Power vs Voltage and Current vs Voltage graph*

3.1.3 Relationship between duty cycle and input voltage

Fig. 5 shows analysis plots Duty Cycle against input voltage (Vin) to evaluate how the Perturb and Observe (P&O) algorithm adjusts the boost converter's duty cycle to track the Maximum Power Point (MPP). The x-axis shows Vin from 10V to 48V, covering the simulated PV panel's range, while the y-axis displays Duty Cycle, rising from 100 to 196 from Steps 1–34, then dropping to 172 from Steps 35–40. From 10V to 20V (Steps 1–12), the Duty Cycle increases from 100 to 140 as power rises, showing good MPP tracking. After 20V (Step 13), it climbs to 196 by Step 34 despite falling input power (Pin), indicating overshooting, and decreases to 172 from 35V to 48V (Steps 35–40) with no effect as input current (Iin) hits 0A in the open-circuit region. Key insights show the P&O algorithm tracks well up to the MPP (Step 12), but overshooting post-MPP suggests a need for adaptive step sizes to boost efficiency.

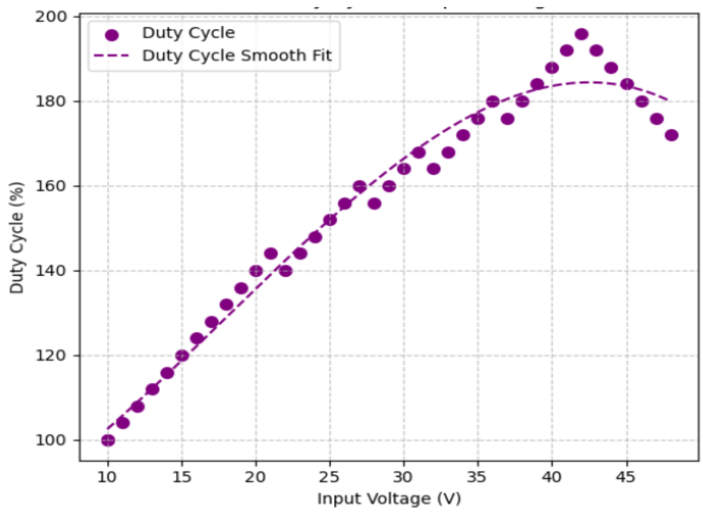

Fig. 5 *Duty Cycle vs Voltage graph*

3.1.4 Relationship between efficiency and input voltage

Fig. 6 shows analysis plots efficiency, calculated as (Pout/Pin × 100%), against input voltage (Vin) to evaluate the MPPT system's power conversion effectiveness. The x-axis shows Vin from 10V to 48V over 40 steps, covering the

PV panel's short-circuit to open-circuit range, while the y-axis displays efficiency, set to 0% when Pin = 0 to avoid errors. From 10V to 20V (Steps 1–12), efficiency ranges from 96% to 88%, peaking at 100% at Step 4, showing good MPP tracking. After 20V (Step 13), it drops to 57% and fluctuates, hitting 410% at Step 33 due to low Pin (1W) and high Pout (164W), a simulation artifact from the boost converter, then falls to 0% at Steps 34–40 as Pin = 0W. Key insights reveal high efficiency (88%–100%) near the MPP (20V–26V) confirms effective tracking, but post-MPP anomalies over 100% highlight simulation limits, suggesting a cap at 100% or better control in low-power areas for improved reliability.

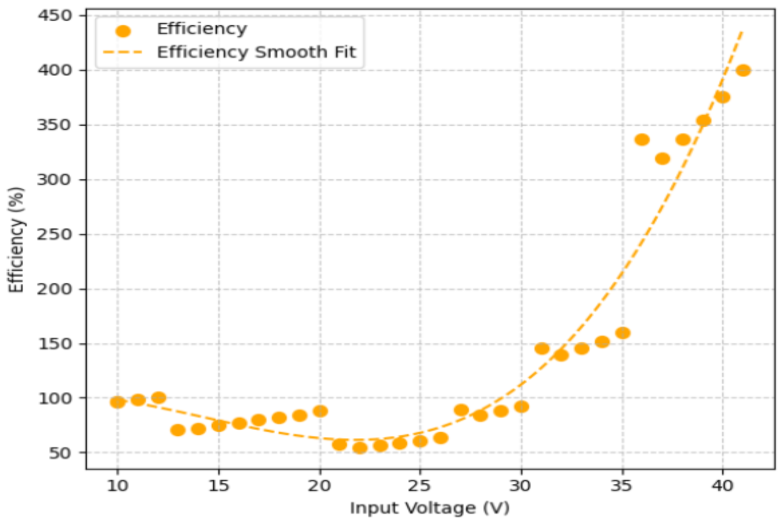

Fig. 6 *Efficiency vs Voltage graph*

4 Conclusion

This project successfully meets all objectives with the proposed system has high efficiency, despite some post-MPP simulation artifacts; and the third, evaluating performance via RTL simulation with Quartus II and ModelSim. For improvements, an adaptive step size to reduce MPP oscillations, might improve the proposed system that reflect the real-world usage.

Acknowledgement

The authors would like to express the deepest gratitude to the Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia for the logistic support.

Conflict of Interest

Authors declare that there is no conflict of interest regarding the publication of the paper.

Author Contribution

The authors confirm contribution to the paper as follows: ***study conception and design:*** *Abdul Sabiq Bin Mohamad Ramli;* ***data collection:****Abdul Sabiq Bin Mohamad Ramli;* ***analysis and interpretation of results:*** *Abdul Sabiq Bin Mohamad Ramli;* ***draft manuscript preparation:*** *: Abdul Sabiq Bin Mohamad Ramli, Intan Sue Liana Binti Abdul Hamid. All authors reviewed the results and approved the final version of the manuscript.*

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