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Energy Efficient Arithmetic Logic Unit (ALU) Based On Dynamic Voltage And Frequency Scaling (DVFS)

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Abstract: This project presents a design of 8-bit Arithmetic Logic Unit (ALU) with eight different operations. ALU is the most crucial parts in digital computer which is designed to compute all the arithmetic and logic operations, including decoding operations that need to be done for almost any data that is being processed by the central processing unit (CPU). In the applications of digital circuits, there are some important attributes that need to be considered such as maximizing speed and minimizing power consumption. Higher power consumption results in more heat dissipation, higher cooling cost and make the system more prone to failures and malfunctions. Therefore, this project will cover in designing 8-bit ALU with eight operations by using Intel Quartus Prime Development Suite. Verifying the functionality and performance of ALU that implement DVFS technique and optimizing the performance of ALU in term of frequency, timing, and power by maximize power saving. This project will focus on three conditions which are high performance, optimized, and low performance test. The integrations of all sub-modules will create an efficient and effective solutions for ALU design. The generated graph from Maple proves the DVFS technique. DVFS technique improved by 25% from the conventional technique in term of timing performance.

Keywords: System Performance, Energy, Power Reduction, Power Saving Technique

1. Introduction

This project paper presents a design of 8-bit ALU with eight different operations. ALU is the most crucial parts in digital computer which is designed to compute all the arithmetic and logic operations, including decoding operations that need to be done for almost any data that is being

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processed by the central processing unit (CPU) [1]. In the applications of digital circuits, there are some important attributes that need to be considered such as maximizing speed and minimizing power consumption. Higher power consumption results in more heat dissipation, higher cooling cost and make the system more prone to failures and malfunctions [2]. However, low power consumption literally can reduce the problems related to heat and also reduced the performance of the system [3]. Therefore, this project will cover in designing 8-bit ALU with eight different operations by using Intel Quartus Prime Development Suite. Next, determining optimize voltage and frequency by using Maplesoft Maple. Verifying the functionality and performance of ALU that implement DVFS technique and optimizing the performance of ALU in term of frequency, timing, and power by maximizing power saving. This project will focus on three conditions which are high performance, optimized and low performance test. The integrations of all sub-modules will create an efficient and effective solutions for ALU design. The generated graph from Maple proves the DVFS technique.

2. Prior Work

There was an approach to reduce power constraint test time by finding the best voltage and frequency which was run by Venkataramani, Sindia, and Agrawal [3] which measure the maximum frequency for a circuit with peak power per cycle for a given supplied voltage. Altera DE2 Field Programmable Gate Array (FPGA) board is the circuit used for measurements and a benchmark circuit is programmed on that particular board. Maximum test frequency and peak power per cycle plotted as a function of the supplied voltage. Since the DE2 board includes a number of peripherals, such as a seven-segment display, several LEDs, various input/output drivers, etc. These peripheral components will dominate the absolute power numbers measured from the supply voltage and current product, rather than the actual circuitry on the board. By eliminating in each cycle, the steady state power component, the measured supply-power can be corrected. CMOS circuitry on the FPGA presumably dominates the remaining power component, which is the switching power. Square of the supply voltage in the range of 1.8V – 5.4V, the peak dynamic power per cycle increases which is goes equally with theory. Even very low-test requirements result in erroneous results for supply voltages below 1.8V, which is plausible, since the nominal voltage specified for the FPGA board is 3.3V, and one or more IO drivers may not be operational at voltages below 1.8V. Even though the nominal voltage commonly used for CMOS logic circuits at the 90nm technology node is around 1.2V, the supply voltage to the DE2 board can be control in the range 1.8V to 5.4V.

3. Results and Discussion

In order to justify the optimized supplied value voltage from the simulation testing, theoretical calculation regarding DVFS technique has to be made. This will make sure the obtained value from the simulator is at least almost accurate with theoretical calculations. First, the total switched capacitance, *CL* needs to be calculated. It consists of three basic parameters which are power, voltage and frequency. The power is divides with the square of voltage which multiplied with frequency. By combining and arranging all of the parameter, the equation can be seen as below:

$$CL = Power\ Voltage^2\ x\ Frequency$$

Next, the maximum energy dissipated, *Emax* is calculated by multiplying the total switched capacitance that obtained before with the square of supplied voltage. The arrangement of the equation can be simply seen as:

$$E_{max} = CL\ x\ VDD^2$$

After that, test clock cycle period at peak power, *Tpower*, need to be calculated. Calculating clock cycle is just by simply divide 1 by the frequency which can be seen as below:

$$Tpower = 1/\ fmax$$

Since the value of maximum energy dissipated and test clock cycle period at peak power has been obtained, the next step of calculating this technique can be proceed by calculating the peak power of the circuit, *Pmax*. *Emax* is divided with *Tpower* which will produce *Pmax*. The arrangement of the equation can be simply seen as:

$$Pmax = Emax\ Tpower.$$

The results are obtained from the waveforms, and timing simulation data which are simulated using Intel Quartus Prime Development Suite tools. The propagation delay of the ALU is measured from the waveforms, while the value of total thermal power dissipation in the ALU can be obtained from the PowerPlay Power Analyzer Tool. As for the timing for the design, it was obtained from the Timing Analyzer.

From the preliminary results, DVFS technique can be applied by using all of the related formulas and optimized voltage can be obtained. Then the optimized voltage was simulated again in the Intel Quartus Prime Development Suite again by using the same ALU design created previously. After that, all of the required parameters were obtained and compared with the conventional ALU design.

Table 1: Functional Simulation of Proposed Design

En	1
Input A	00001010
Input B	00000101
Add	00001111
Logicand	00000000
Logicnand	11111111
Logicnor	11110000
logicnot	11110101
Logicor	00001111
Logicxor	00001111
Sub	00000101

The timing simulation waveform can be obtained from logic XOR operation. Even though this simulation is being tested from XOR operation, other operation will produce the same maximum timing as well. When $En = 1$, $Input\ A = 00001011$, $Input\ B = 00000101$ and $Operation = 111$, the generated output $logicxor = 00001110$ will be shown.

Maximum timing of 17.22ns obtained from the waveform. From this value, maximum clock frequency, f_{max} can be automatically obtained by using the following formula.

$$f_{max} = \frac{1}{t_{max}}$$

By applying the formula, f_{max} will be 58.072 MHz.

By running PowerPlay Power Analyzer Tool from the Intel Quartus Prime Development Suite, core static thermal power dissipated, and I/O thermal power dissipated can be obtained. This two-power dissipation can be combined together in order to obtain the total thermal power dissipation. This feature also can simulate the computed junction temperature, thermal power dissipation by block type and hierarchy of the proposed design. From that, the difference of total thermal power dissipation can be analysed clearly where conventional ALU design consumes 170.41 mW while ALU design with DVFS consumes 170.24 mW.

In order to obtain the optimize supply voltage for the circuit design created, all of the parameters obtained from the simulator were considered. To generate a graph that shows test time against supply voltage, Maple 2019 was used. Since the simulation software set the default frequency to 1,000 MHz,

the calculation will be made in two categories which are default frequency (1,000 MHz) and actual frequency (437.5 MHz).

Table 2: Parameter Values for ALU Circuit Design

Parameter	Value
Power	170.41 mW
Voltage	1.2 V
f_{power}	1,000 MHz
t_{max}	17.22 ns
f_{max}	58.072 MHz
V_{TH}	0.26 V
C_L	2.0378 nF
K	4.3476×10^{-10}
α	2

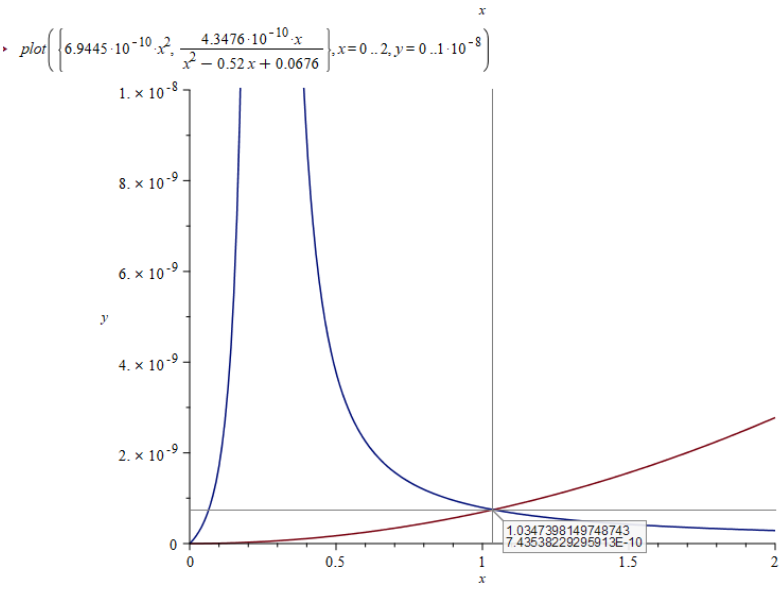

Figure 1: Simulated curve by applying test time equations at various voltages.

In theoretical Frequency will increase and timing will decrease which is the relationship is vice versa. Some calculations were made so that the values obtained from simulation is justified.

$\gamma = \left(\frac{K \times P_{max}}{C_L}\right)^{\frac{1}{\alpha}}$:

$\gamma = 0.79122$

$V_x{}^{\alpha+1} - V_{TH} \cdot V_x - \gamma = 0$

$V_x = 1.01832$

$V_x = V_{DD}^{\frac{1}{\alpha}}$

$V_{DD} = 1.03697$

$T_{opt} = \frac{K \times V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$

Proportionality Constant, K ($\times 10^{-9}$)	Maximum Switched Capacitance C_L (nF)	Peak per cycle power, P_{max} (W)	Nominal Voltage Test (1.2V)		Optimum voltage test			Test time reduction (%)
			Test Clock frequency (MHz)	Test time (ns)	Supply Voltage	Test Frequency, f_{opt} (MHz)	Test time (ns)	
0.43475	2.0378	2.9344	1,000	1	1.037	1.3391	0.74675	25

$T_{opt} = 0.74675 \times 10^{-9}$

$f_{opt} = \frac{1}{T_{opt}}$

$f_{opt} = 1.3391 \times 10^{9}$

Table 3: Comparison Between Nominal Voltage Test and Optimum Voltage Test for Default Frequency

For the conventional ALU, the core voltage is 1.2 V while ALU that implement DVFS technique is 1.0V. Both simulations were conducted with the same family device with the same applied technology which is Cyclone IV E. By using the same family device, the results will be more precise.

Since the simulation software set the default frequency to 1,000 MHz, another calculation was which the frequency is calculated based on actual frequency (437.5 MHz).

Figure 2 shows the generated graph from the preliminary result for actual frequency. The optimized voltage supply value can be seen clearly as the equations of test time intersect each other. From that intersection, there are two important parameter values are obtained which are the optimized voltage supply value and also the test time for the circuit when optimized voltage is applied.

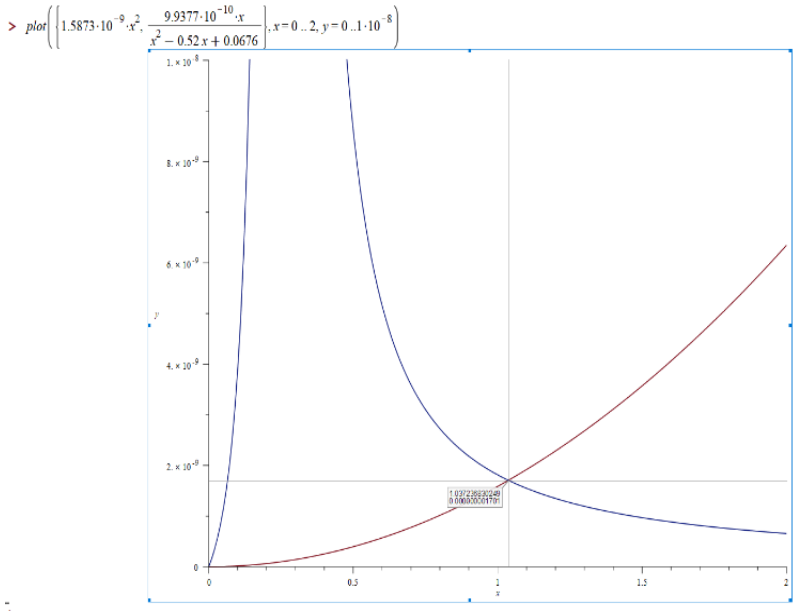

Figure 2: Simulated curve by applying test time equations at various voltages.

In theoretical Frequency will increase and timing will decrease which is the relationship is vice versa. Some calculations were made so that the values obtained from simulation is justified.

$$\gamma = \left(\frac{K \times P_{max}}{C_L}\right)^{\frac{1}{\alpha}}$$

$$\gamma = 0.7912$$

$$V_x{}^{\alpha+1} - V_{TH} \cdot V_x - \gamma = 0$$

$$V_x = 1.0183$$

$$V_x = V_{DD}{}^{\frac{1}{\alpha}}$$

$$V_{DD} = 1.03697$$

$$T_{opt} = \frac{K \times V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

$$T_{opt} = 1.7069 \times 10^{-9}$$

$$f_{opt} = \frac{1}{T_{opt}}$$

$$f_{opt} = 585.8574 \times 10^{6}$$

Table 4: Comparison between Nominal Voltage Test and Optimum Voltage Test for Default Frequency

Table 4 shows the comparison between the results of nominal voltage which is 1.2 V and optimum voltage which is 1.037 V. The clock frequency is increased as the clock frequency for nominal voltage is 437.5 MHz and optimum voltage is 585.9547 MHz. Since the frequency is increased, the test time is decrease which as for nominal voltage is 2.2857 ns and optimum voltage is 1.7069 ns. This can be concluded by reduce the value of voltage supply, the test time can be reduced up to 25.32%.

4. Conclusion

In a nutshell, the integrations of addition, subtraction operations with the logic operations will create an efficient and effective solution for ALU design. Each of the operations are design specifically in order to compute the desired output. As for the latch, it operates as an activator since it produces an output that follows the input whenever the enables are 'HIGH' so that all operations are not run at the same time. This is one of the ways to reduce power consumption of the design by activating the only necessary operations in order to produce desired output. The integrations of all the systems to be a single top module successfully design an 8-bits ALU with eight operations by using Intel Quartus Prime Development Tools. The calculation of optimize voltage and frequency applies all of formulas related to DVFS technique. At first, the total switched capacitance was calculated so that the maximum energy dissipated by the clock cycle of the design can be obtained. From that, peak power can be obtained by dividing maximum energy with clock period at a selected peak power. All of these obtained parameters were applied on the test time formula and a line graph was obtained which shows the optimized value for the system. The optimized voltage and frequency were determined by using Maplesoft MAPLE. The functionality and performance of ALU that implement DVFS method was verified by using Intel Quartus Prime Development Tools where all of the operations were run and checked. The optimized supplied voltage for both default frequency and actual frequency is 1.037 V. There is only difference at the optimum test frequency where on default frequency, the optimized frequency is 1.3391 MHz while for actual frequency is 585.8574 MHz. The obtained frequency value leads to the optimized test time where 0.7467 ns for the default frequency and 1.7069 ns for actual frequency. All of the obtained results achieve all of the targeted objectives and creates an effective ALU design with variety of performance in term of timing, frequency, and power.

Proportionality Constant, K ($\times 10^{-9}$)	Maximum Switched Capacitance C_L (nF)	Peak per cycle power, P_{max} (W)	Nominal Voltage Test (1.2V)		Optimum voltage test			Test time reduction (%)
			Test Clock frequency (MHz)	Test time (ns)	Supply Voltage	Test Frequency, f_{opt} (MHz)	Test time (ns)	
0.99377	2.0378	1.2838	437.5	2.2857	1.037	585.8574	1.7069	25.32

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