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Analysis of I-V Characteristics of Silicon PIN Diodes

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Abstract

PIN diodes are a special kind of semiconductor that are used widely in microwave and radio frequency (RF) circuits because they function as current-controlled resistors at these frequencies. This research focuses on simulating the effects of varying intrinsic region widths on the I-V characteristics. The investigation spans a range of intrinsic region widths from 2.5 µm to 175 µm using Sentaurus TCAD to design a silicon PIN diode structure. Results show a consistent decrease in forward current as the intrinsic region width increases. The study provides essential insights for optimizing PIN diode performance in high-frequency applications, validated through comparison with theoretical calculations. The results show that the forward current through the PIN diode decreases as the intrinsic region width increases when compared to theoretical calculations. At a thickness of 2.5 µm, the calculated current value is 2.24 µA, a slightly higher than the simulated value of 2.12 µA. However, as the thickness increases, the difference becomes more noticeable. At 6 µm, the calculated current value rose to 5.38 µA, while the simulated value drops to 1.19 µA. The I-V curves illustrate this relationship, indicating that widening the intrinsic region leads to a reduction in current flow. This finding provides valuable insights for optimizing PIN diode performance in high-frequency applications.

1. Introduction

The PIN diode saw its initial application in 1952 as a rectifier for low frequency and high-power signals. Its usage extended to microwave applications and photodetection, owing to its reputation as an effective light absorber (Bhakti, 2023). A PIN diode represents a progression from the conventional PN combination diode. It consists of three layers, wherein an intrinsic section, i.e., an undoped semiconductor, is sandwiched between N and P regions, thus defining it as a PIN diode. The intrinsic region serves as the high-resistance section, leading to an elevation in the magnitude of electric flux (Bhakti, 2023). The PIN diode is different from essentially a PN junction because it consists of a lightly doped semiconductor layer termed as which a high-resistivity intrinsic region sandwiched between P-type and N-type semiconductor region. The existence of intrinsic region in PN junction make it ideal for such as radio frequency (RF) switching, microwave attenuators, photodetectors, and fast electronics switches (Doherty, n.d.). PIN diode has wide applications only because of the intrinsic layer. The intrinsic region comprises of the undoped or virtually undoped semiconductor and in most PIN diodes, the width is very thin and varies between 5 µm and 200 µm. PIN diode is a current controlled resistor at radio and microwave frequencies. The existence of intrinsic region in PN junction make it ideal for such as radio frequency (RF) switching, microwave attenuators, photodetectors, and fast electronics switches.

As the intrinsic region's thickness changes, it affects the flow of electrons and positive holes within the diode. The work aims to analyze how this variation influences the I-V characteristics, which represent the

relationship between current and voltage in the diode. When a forward bias is applied to a PIN diode, electrons and positive holes are introduced into the intrinsic region. This alters the resistivity of the intrinsic region, leading to changes in the high-frequency series resistance. Investigating these changes provides valuable insights into how the PIN diode behaves under different conditions. Because of its ability to withstand high voltages in their middle layer, PIN diodes are also utilized in power electronics. The current passing through a PIN diode when it is turned on determines its resistance (Othman, 2014). The middle part of the diode, called the intrinsic region, has a resistance that changes with the amount of electrons and positive holes in it. This variation affects the resistance at high frequencies. The intrinsic region is what makes the PIN diode different from a regular diode (Microsemi Watertown, 1993). This work aims to explore the effect of different inner layer thickness on the I-V characteristics of a silicon PIN diode. Sentaurus TCAD, could model a PIN diode with different intrinsic region width thicknesses. To compare the simulation results with calculations to find the effect of different intrinsic region width.

2. Methodology

An overview flow of the design and analysis process for PIN diodes is shown in Fig**.** 1.

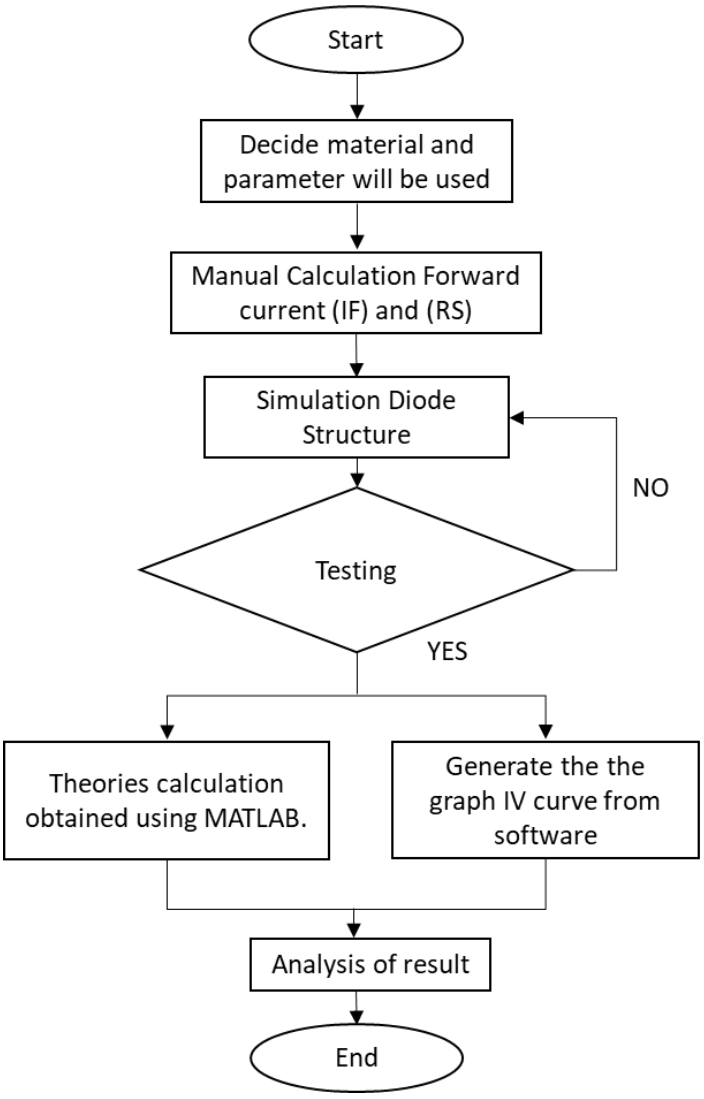

Fig. 1 *Whole flowchart of the work*

2.1 Device Structure

Sentaurus Device Editor can be used as a two-dimensional (2D) or three-dimensional (3D) structure editor, and a 3D process emulator to create TCAD devices. A simulation of the SDE is used in the design process of silicon PIN diodes (Sentaurus Visual User Guide, 2013). Fig. 2 shows a 2D diagram of a PIN diode. The length of each structure PIN diode is depended on intrinsic region widths for the thickness for P-type and N-type layer is 10 µm (Jubadi & Noor, 2010). The device using silicon material semiconductor substrate consists doping of 1017 cm3

boron on P-type region and heavily doped of phosphorus with 1019 cm3 on N-type region. Have also thin layer of oxide of 0.3 µm is grown. The I-V characteristics at 2.5 µm, 5 µm, 15 µm, 25 µm, 45 µm, and 175 µm have been analyzed using six different widths. With a voltage range of -10 V to 10 V, the simulation solely takes into account the forward bias situation.

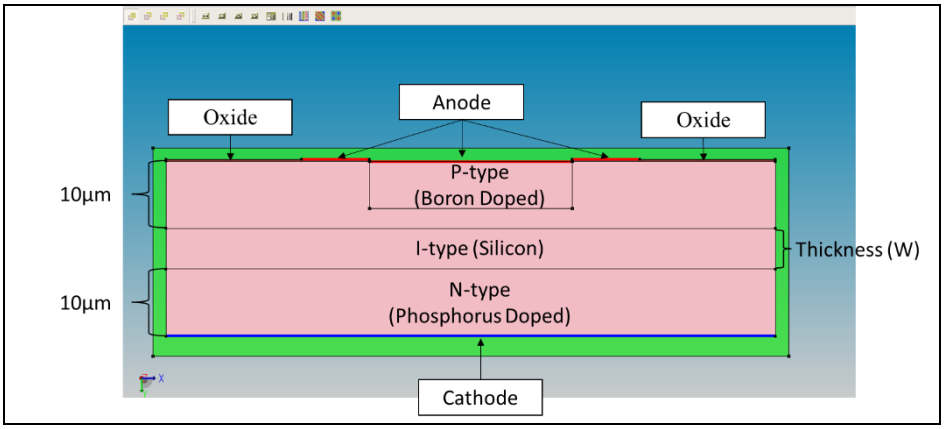

Fig. 2 *Structure of Silicon PIN diode*

2.2 Parameter for PIN Diode Design

As mentioned earlier, the calculation was performed to obtain the IV value manually. From this calculation, can compare the results with the I-V curve from the Sentaurus tool. In this work, the parameters listed in Table 1 is used (Bhattacharyya, 2019).

Table 1 *Parameter for PIN diode design*

Parameter	Value
Total number of donor atoms/cm^3 ,N_D	10^{19}
Total number of acceptor atoms/cm^3 ,N_A	10^{17}
Concentration of silicon at 300K, n_i (cm^{-3})	1.5×10^{10}
Minority carrier lifetime , τ (s)	10^{-6}
Temperature, T (K)	300
Permittivity of free space (ε_0) (F/cm)	8.85418×10^{-14}
Diode area, A (cm^2)	10^{-4}
Boltzmann's constant, k (J/K)	1.3806×10^{-23}
Electron diffusion constant, D_n (cm^2/s)	39
Hole diffusion constant, D_p (cm^2/s)	12

3. Result and Discussion

Calculation and simulation results are compared to conduct analysis. In this part, a PIN diode structure was simulated by using the Sentaurus Structure Editor for various intrinsic region widths of 2.5 µm -175 µm obtained results were shown. Since the thickness of the P-type and N-type layers is 10 µm, the length of each structure PIN diode depends on the intrinsic region widths. Silicon material semiconductor substrate is used in the device, which is extensively doped with phosphorus (1019 cm3) on the N-type area and boron (1017 cm3) on the P-type region. furthermore, generated a 0.3 µm thin layer of oxide. Set contact on the PIN diode, the top part is the anode and the bottom part is the cathode. This is the device structure with its current meshing and doping condition, viewed in Tecplot-Sentaurus.

3.1 Doping Mesh Simulation Result

In Fig. 3 – 8, the diagram displays the doping profile of a PIN diode. The I-region has a width of 2.5 µm-175 µm, while the overall length of the diode is set at 90 µm. The P-type and N-type layers, representing the top and bottom parts, have a thickness of 10 µm each. This illustration provides insight into the size and placement of the various components in the diode.

3.1.1 2.5 µm I-region Width

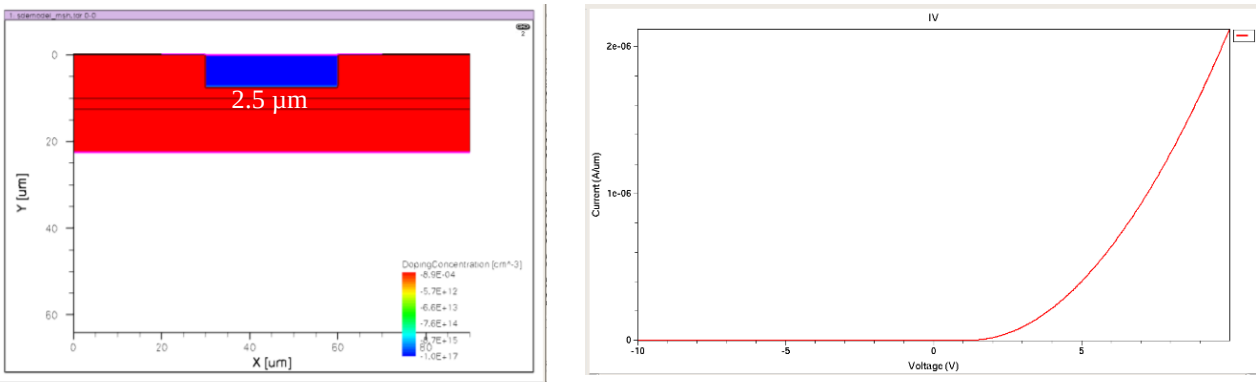

Fig. 3 *Simulation the doping profile and I-V characteristics of a PIN diode with I-region width 2.5 µm. The length is set at 90 µm and thickness for the P-type Boron (10^{17} cm^3) and N-type layer (10^{19} cm^3) is 10 µm. The highest current (IF) is 2.12 µA, and the diode begins operating at a current of 1.8x10^{-2} µA.*

3.1.2 6 µm I-region Width

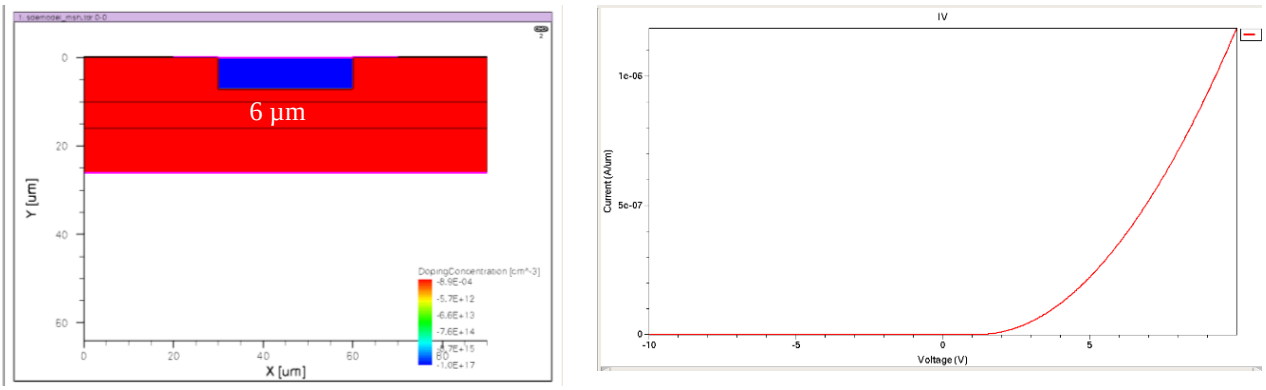

Fig. 4 *Simulation the doping profile and I-V characteristics of a PIN diode with I-region width 6 µm. The peak current I_F is 1.12 µA, and the diode becomes operational at a current of 1x10^{-2} µA.*

3.1.3 15 µm I-region Width

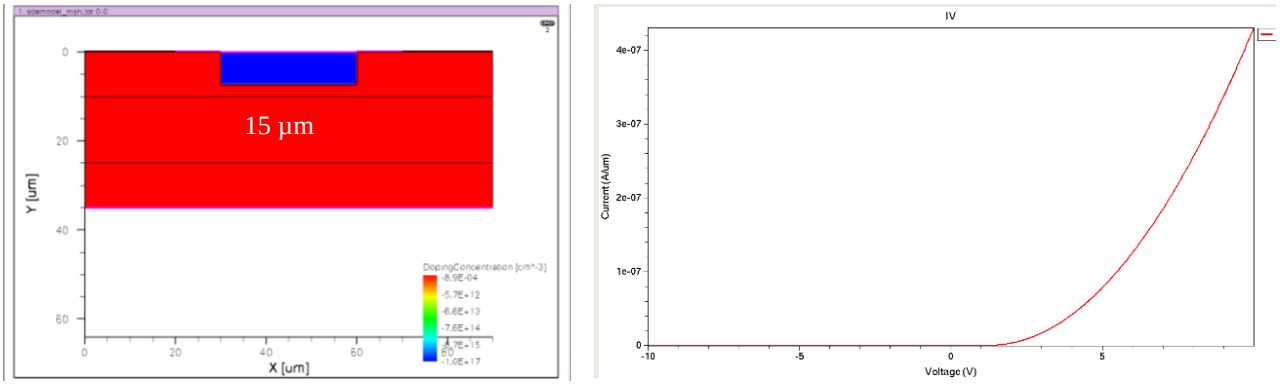

Fig. 5 *Simulation the doping profile and I-V characteristics of a PIN diode with I-region width 15 µm. The peak I_F is at 0.43 µA and the I_F for the diode to start operational is at 3.43x10^{-3} µA.*

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3.1.4 25 µm I-region Width

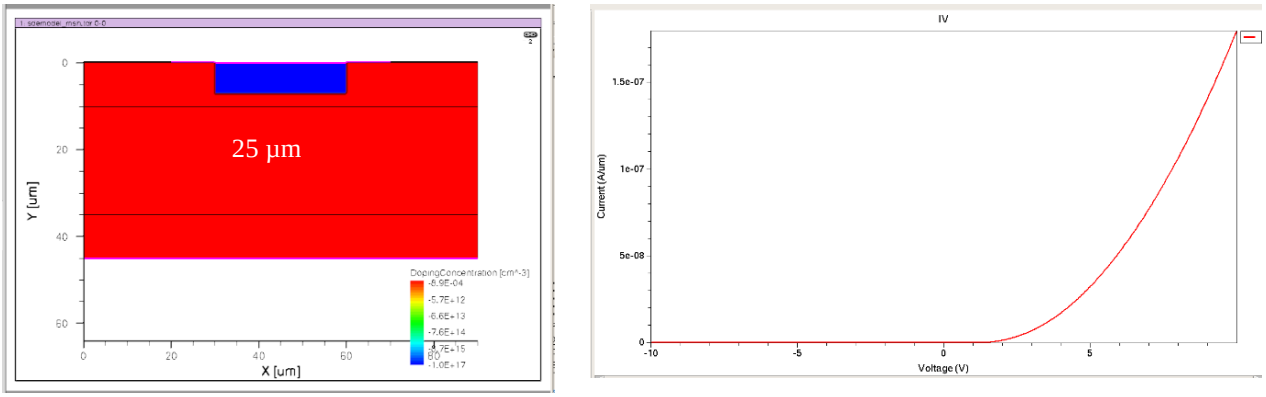

Fig. 6 *Simulation the doping profile and I-V characteristics of a PIN diode with I-region width 25 µm. The peak I_F is at 0.18 µA and the I_F for the diode to start operational is at 1.3x10^{-3} µA.*

3.1.5 45 µm I-region Width

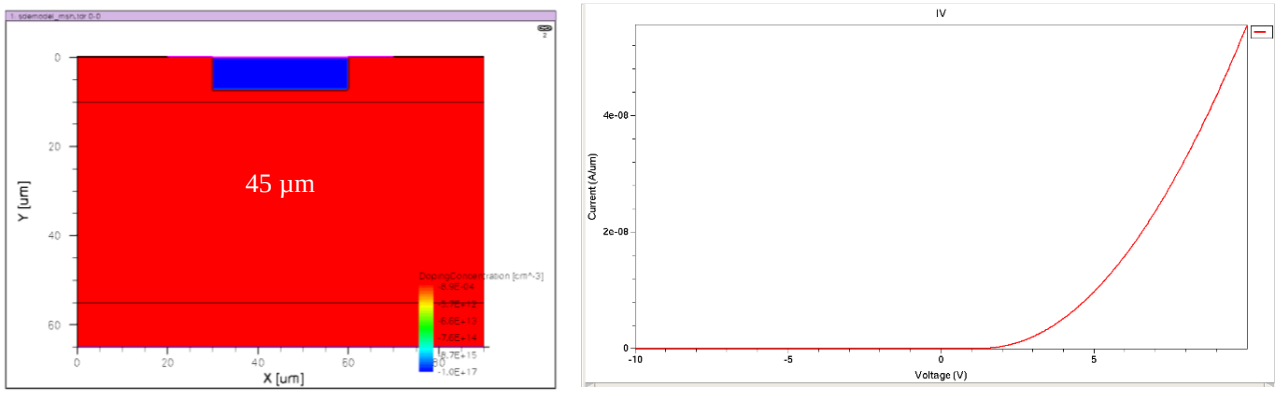

Fig. 7 *Simulation the doping profile and I-V characteristics of a PIN diode with I-region width 45 µm. The peak I_F is at 0.06 µA and the I_F for the diode to start operational is at 3.66x10^{-10} A.*

3.1.6 175 µm I-region Width

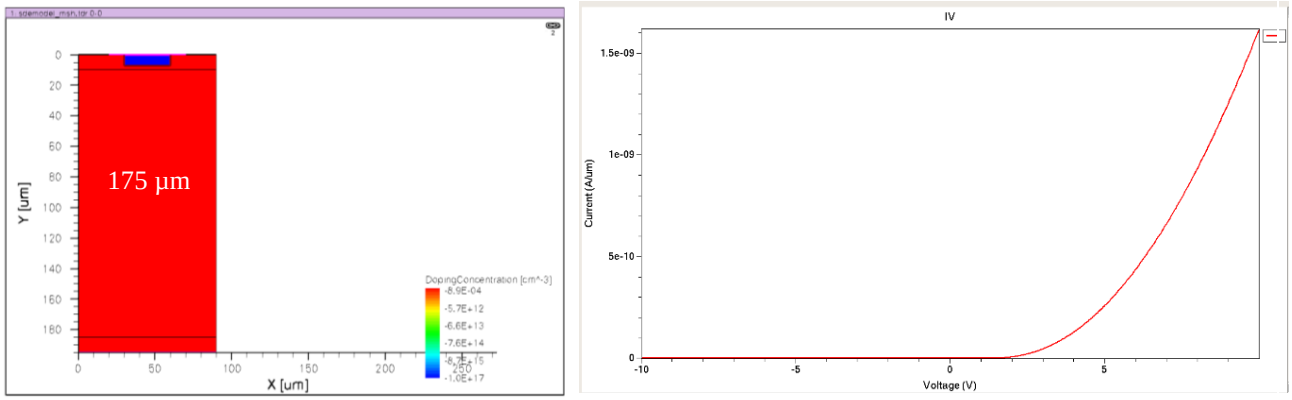

Fig. 8 *Simulation the doping profile and I-V characteristics of a PIN diode with I-region width 175 µm. The peak I_F is at 0.002 µA and the I_F for the diode to start operational is at 6.45x10^{-12} A.*

Figure 3 – 7 display six different curves (I-V curves) representing various widths of the intrinsic region in a PIN diode. Each curve illustrates how the current changes relative to the applied voltage for different intrinsic region widths. The graph indicates that as the width of the silicon PIN diode increases, the current decreases. Furthermore, it is clear that the current flow reduces as the thickness of the intrinsic area increases. Put another way, the current in the PIN diode drops as the thickness of the intrinsic area grows. In the simulation, when 10 V

is applied, the 175 µm-wide silicon PIN diode barely permits 0.097 µA of current to pass. On the other hand, the silicon PIN diode of 2.5 µm has the highest current flow, reaching up to 136 µA at the same voltage. Conversely, the thickness of the intrinsic region narrows, as the current increases.

4. Analysis and Discussion

Fig. 9 displays six different curves (I-V curves) representing various widths of the intrinsic region in a PIN diode. Each curve illustrates how the current changes relative to the applied voltage for different intrinsic region widths. It can be seen from the graph that current drops with increasing silicon PIN diode width. Additionally, it is evident that when the intrinsic region's thickness widens, the current flow decreases. In other words, as the thickness of the intrinsic region increases, the current in the PIN diode decreases. The simulation indicates that when powered by 10V, the 175µm-wide silicon PIN diode allows a current flow of just 0.097µA. Conversely, the silicon PIN diode, which has a 2.5µm width, has the most current flow at the same voltage, with a maximum of 136µA. Conversely, the thickness of the intrinsic region narrows, as the current increases.

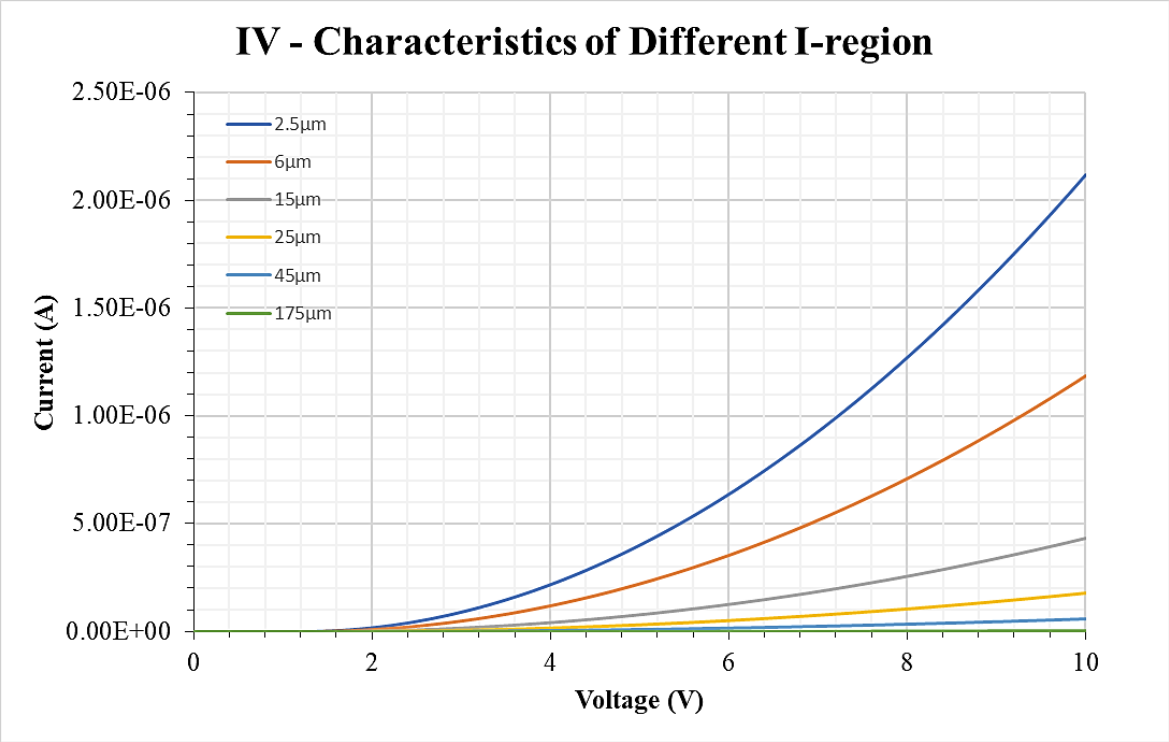

Fig. 9 *Combination of I-V Curve with a different intrinsic region width.*

4.1 Theories Formula

To find the generation-recombination current:

$$I_{GR} = \frac{qAWn_i}{2\tau} \tag{1}$$

where:
A= Surface area of PIN diode
W= Depletion width

To find the pre-factors to the generation-recombination current:

$$I_0 = qA\left(\frac{D_P p_n}{L_P} + \frac{D_n n_p}{L_n}\right) \tag{2}$$

To find the current:

$$I_F = I_O\left(\exp(Vt \times V) - 1\right) + I_{GR}\left(\exp(Vt \times V) - 1\right) \tag{3}$$

where:
V= bias voltage

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By using Equation (1) - (3), with a temperature of 300 K and a bias voltage of 0.3 V, the currents for various widths are computed. Table 2 provides a summary of the findings. Through computer modeling, we found that increasing the width of a Silicon PIN diode reduces its current performance. then matched these findings to P-N junction computations as both have a similar intrinsic region behavior. The reliability of the current-voltage (IV) curve was confirmed through these calculations. In Table 2, simulated and calculated maximum forward current (I_F) values is compared. To calculate the current in the PIN diode, we used formulas related to its minority charge density, the intrinsic region, minority diffusion length, and generation-recombination current.

Table 2 *Comparing Forward Current (I_F) in Simulation and Calculation*

Thickness (μm)	Calculated Current (μA)	Simulated Current (μA)
2.5	2.24	2.12
6	5.38	1.19
15	0.13	0.43
25	0.22	0.18
45	0.4	0.06
175	0.016	0.002

4.2 Maximum Forward Current (I_F)

Fig. 10 shows the biggest forward current, I_F, against the width of the intrinsic region. The results for the maximum forward current, I_F, are marked on the I-V simulation. When the intrinsic region width gets bigger, the forward current goes down. So, in simple terms, I_F and the intrinsic region width are kind of like opposites when one goes up, the other goes down. This happens because the intrinsic region probably has a lot of resistance on its own.

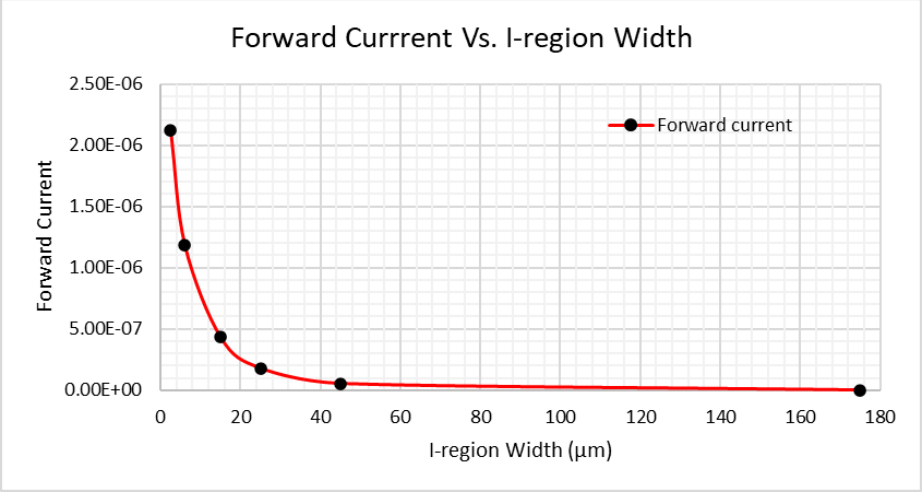

Fig. 10 *Forward Current versus the width of the I-region.*

5. Conclusion

To sum up, the first objective of this study is to design the Silicon PIN diode with varying intrinsic region width. Next, the second objective is to investigate the effect of varying intrinsic region width of a Silicon PIN diode forward current. The last objective is to analyze the I-V characteristics and compare with the theoretical calculations and simulation results. Basically, in this study, intrinsic region widths effects of the Silicon PIN diode on its I-V characteristics have been successfully verified. Different variations of intrinsic region widths at 2.5 μm, 6 μm, 15 μm, 25 μm, 45 μm and 175 μm also were designed using the Sentaurus TCAD software. Hence, the current performance is inversely proportional to the intrinsic region thickness. From this work, it can be concluded that the suitable width for intrinsic region working at high frequency is 2.5 μm. In general, as the intrinsic region in PIN diode is reduced, device performance in terms of current drive will improve.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The authors confirm contribution to the paper as follows: ***study conception and design:*** *Nur Niwina Nasir, Warsuzarina Mat Jubadi;* ***data collection:*** *Nur Niwina Nasir;* ***analysis and interpretation of results:*** *Nur Niwina Nasir;* ***draft manuscript preparation:*** *Nur Niwina Nasir, Warsuzarina Mat Jubadi. All authors reviewed the results and approved the final version of the manuscript.*

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