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VLSI Implementation of Low Power Face Detection System

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Abstract: This study explores the implementation of a face detection system utilizing Very Large Scale Integration (VLSI) method in improving the low power requirement of the system. Previously, the focus of VLSI was on the area constraints and timing. However, power consumption was becoming more important when the equipment density increases dramatically. When the threshold voltage decreases, the leakage current increases. High power consumption can cause various problems, such as increasing product cost, reducing reliability and reducing battery life. With the help of Electronic Design Automation (EDA) tools, circuits with low power consumption can be designed and at the same time minimized the area. This study is focused on VLSI design flow from Register-Transfer Level (RTL) to Graphic Database System II (GDSII). The EDA tools used in this project are Synopsys Design Compiler and Synopsys IC Compiler from logic synthesis to verification process. Power consumption is improved by using a clock gating technique and the design is optimized after the process. The design has passed the design verifications such as timing, area and power and fulfill the objectives of the study.

Keywords: Face Detection System, Low Power, VLSI

1. Introduction

Face detection system is a technology that is able to identify human faces in digital images or a video frame from a video source captured by camera. Face detection is the first step and essential step for face recognition. Face detection system is not only vital for facial recognition function but also for application in several other areas such as biometric system, surveillance system, monitoring system and security system. In microelectronic industry with the invention of transistor, it has opened the way to put the face detection system in a chip or integrated circuit (IC) and with current technology, a low power consuming device can be designed.

In 2007, a Semiconductor Industry Association (SIA) had reported that the semiconductor global sales had reached billions US dollar [1]. From the report, it is known that semiconductor based companies had received high return as these industries are very profitable. ICs have been the heart for many devices used in human daily lives. Computers, personal digital assistant devices, home appliances, smartphones and many other devices rely heavily on ICs to make them smaller and portable.

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For technology development, useful and beneficial relationships and formulae should be included in every field [2]. It has been predicted by Gordon Moore, the Intel Corporation founder, that the number of transistors in an IC will be double every two years [3]. In the fabrication of a Very-Large Scale Integration (VLSI) IC, millions of transistors are packed into a single chip with smaller die size [4]. The VLSI technology has become so advanced today whereby a System-on-Chip (SoC) can be fabricated. In SoC, a whole system can be embedded into a single chip [5]. In recent technology, even SoC with multi-core can be implemented.

An extremely long design turnaround time (TAT) is needed in designing SoC and it is even further longer for a full custom design [6]. However, Electronic Design Automation (EDA) tools are invented to help IC designers to make TAT shorter. Automatic design approaches are the key in EDA tools to minimize the required TAT in designing complex ICs. Static Timing Analysis (STA), Clock Tree Synthesis (CTS), automatic place and route, and gate level optimization are examples of tools that can be used. EDA tools really help the IC designer and it plays an important role in IC design industry.

In this study, the VLSI design flow is used. The design starts from Register Transfer Level (RTL) function where behaviour of the circuit are described in Hardware Description Language (HDL) format. The RTL source code is then converted into optimized gate level netlist in the process called logic synthesis [4]. The optimized gate-level netlist is then converted into geometrical representation of the design which is known as layout in the physical design stage. Lastly, a Graphic Database System II (GSDII) file is created. This file consists of cell references and the geometry parameters of the cells. GDSII files represents the cell geometric shapes completely labelled with text and other important information about the layout [7].

Low power ICs are the demand of today's electronic devices. Many researches have and are still being done in low power IC design [5]. In VLSI circuits, a critical design parameter is power dissipation as it indicates the battery operated devices performance. As the size of chip area decreases and chip density and complexity increases, it is very difficult to design a high performance system or IC which consumes less power. In sub-micron technologies, leakage power and dynamic power consumption must be taken into account as the important design parameter as the total power consumption is contributed significantly by these two especially by the leakage current [8]. To prolong the battery life of portable devices, power reduction of the VLSI circuit in terms of the leakage and dynamic power must be made. This study has designed and developed a low power SoC for face detection system.

2. Methods

VLSI design process in this study consists of two phases that are front-end design and back-end design. For power optimization, a clock gating technique is used.

2.1 Front-end design with synopsys design compiler

The front-end design started with the system specification or called behavioural design. This is the stage where all the specifications of the system to be designed are listed. The specification is then translated into RTL using HDL. The RTL codes are then imported to the EDA tool and in this study it is Synopsys Design Compiler. The Design Compiler will synthesize and optimize the RTL codes into gate-level netlist depending on the constraints given. Time, power and area are the design constraints put on the circuit being designed. The design constraints are used to optimise the gate-level netlist. The technical process is set by the foundry and covers the models for the logic gates, triggers and wire. It is specified in the target unit library and must be provided to the EDA tool in order to execute technology mapping and optimization.

2.2 Back-end design with synopsys IC compiler

In the physical design, gate-level netlist are converted into the layout which is the circuit geometric representation of the standard cells, clock trees, routings, power nets and several other information

2.3 Power optimization method

In this study, a clock gating method is employed. This high-level technique is used to optimize the power consumption. It is a method of reducing dynamic power in which for selected register banks the clock signals are stopped during times when the stored logic does not change its value. This is because most of the dynamic power is coming from the clock tree that is always switching.

3. Results and Discussion

3.1 Result of static timing analysis

A static timing analysis (STA) is run on the designed circuit. This is done to check all paths in the circuit have met the timing constraint. A timing report is generated to ensure no delay that can cause false output. The STA is done before and after the gated clock is inserted and optimized. The result is shown in Table 1. Based on the table, all the values of slack is positive. It means there are no violations occurs. This is the most important information shown in the timing report.

3.2 Result of VLSI design flow

In the design flow, the outcome is a layout of the circuit being designed. Every layout after the process is shown in Appendix A (Figure 1 to Figure 8). The layout must obey the area constraint and the design rules set by the technology process. Verification has been done and the constraint and design rules are met. The area consumed by the circuit is shown in Table 1. The result obtained shows the total area of the circuit after power optimization for front-end and back-end is greater than the value before optimization. This is because gated clock circuits are added to the design in order to reduce power consumption.

3.3 Result of power optimization

For power, Table 1 shows the total dynamic power after optimization is reduced compared to before optimization. These show that the designed circuit is successful in reducing power consumption. Thus the clock gating technique to get low power design has been successfully implemented.

Table 1: Summary of the results

		Before	After
Front-end	Timing Slack	0.09 ns	0.01 ns
	Area	6801.160457 μm^2	7382.233111 μm^2
	Power	3.0991 mW	418.0528 µW
Back-end	Timing Slack	0.27 ns	0.68 ns
	Area	6973.135837 μm^2	7046.009312 μm^2
	Power	1.8330 mW	1.6641 mW

4. Conclusion

A low power face detection system from front-end design to back-end design and power optimization had been successfully designed and implemented. This circuit which is a face detection system is designed using Synopsys Design Compiler and IC Compiler in the design flow. These tools provide design automation that automates the design tasks, including power optimization. Careful analysis on the timing, area and power is done to ensure no timing violation occurs, the area is within the specification and the power consumed is low. A clock gating technique had been used in this design to ensure the design has a low power consumption. However, the insertion of gated clock increases the area. Nevertheless the increased in area is very small as compared to the power reduction. The logic synthesis stage is completed without any violations in timing and design constraints for the circuit. All

parameter became better compared to before optimization process. Hence, performance for the whole design has been improved.

Appendix A

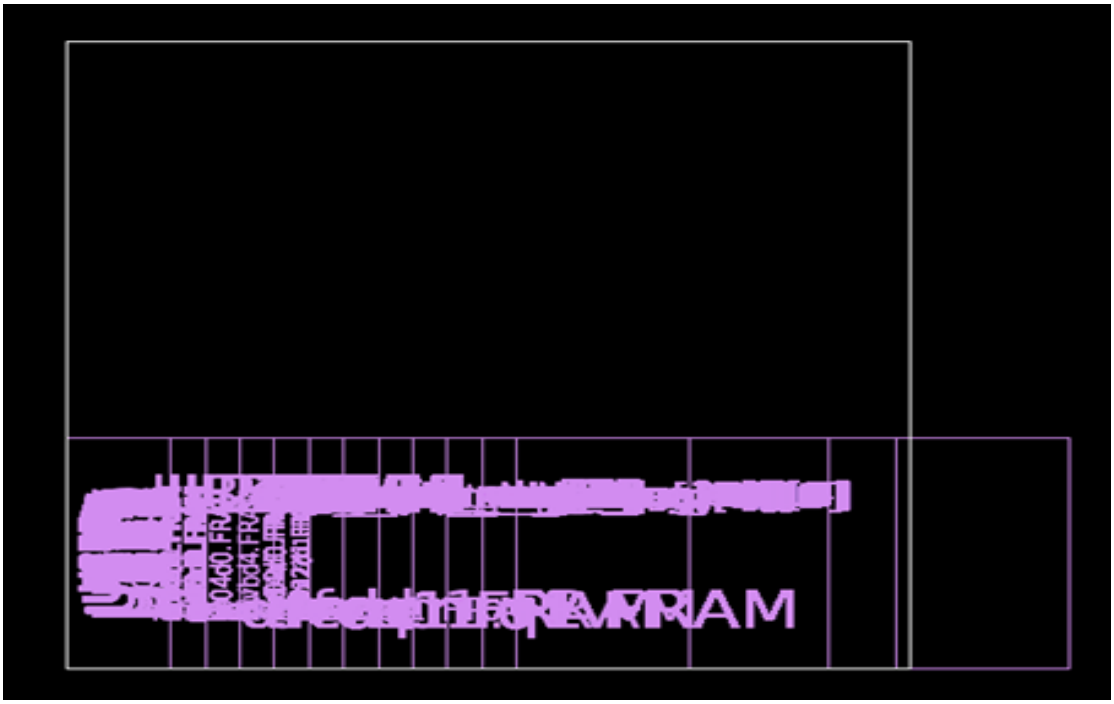

Figure 1: Layout of initial top view cell

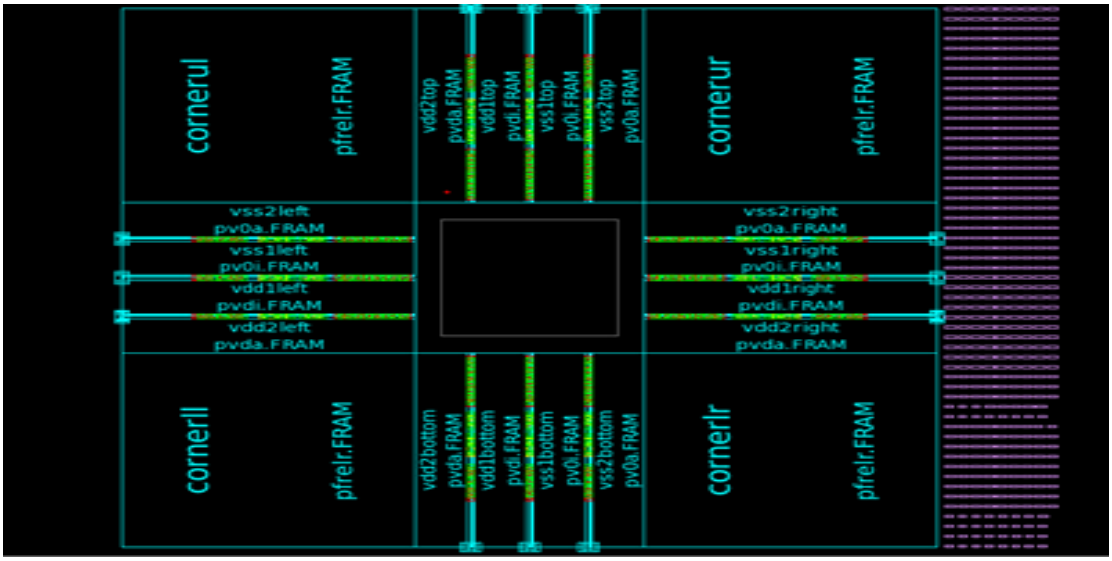

Figure 2: Layout initial floorplan

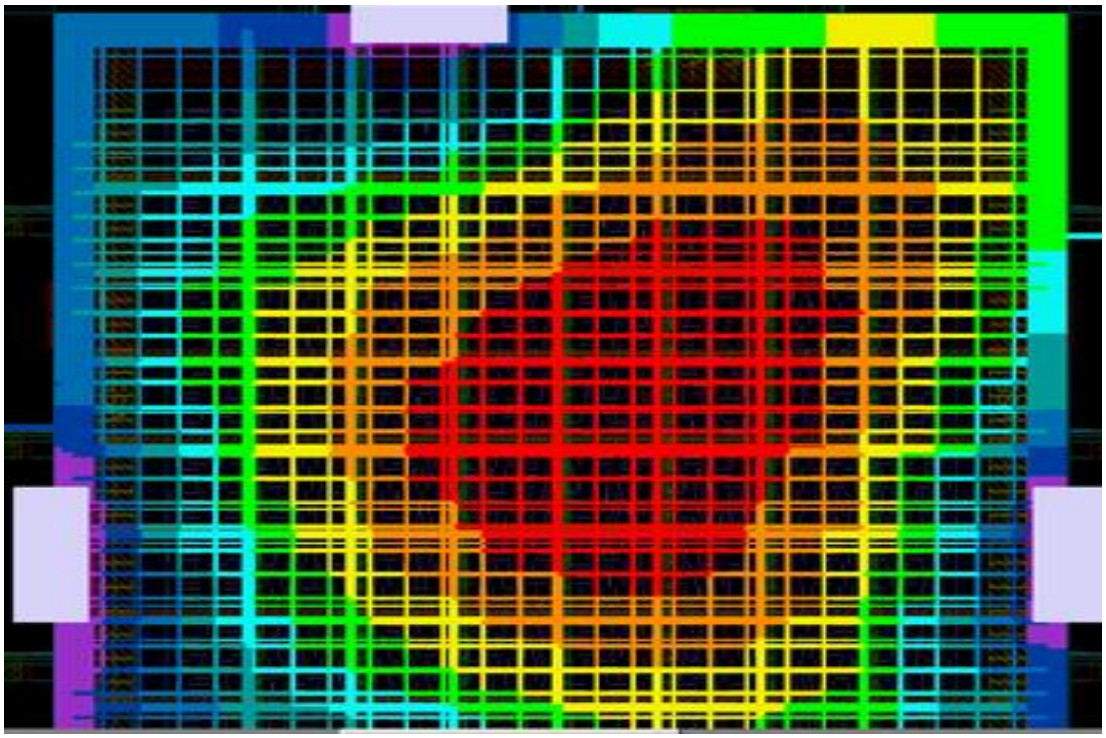

Figure 3: Power map after power network synthesis

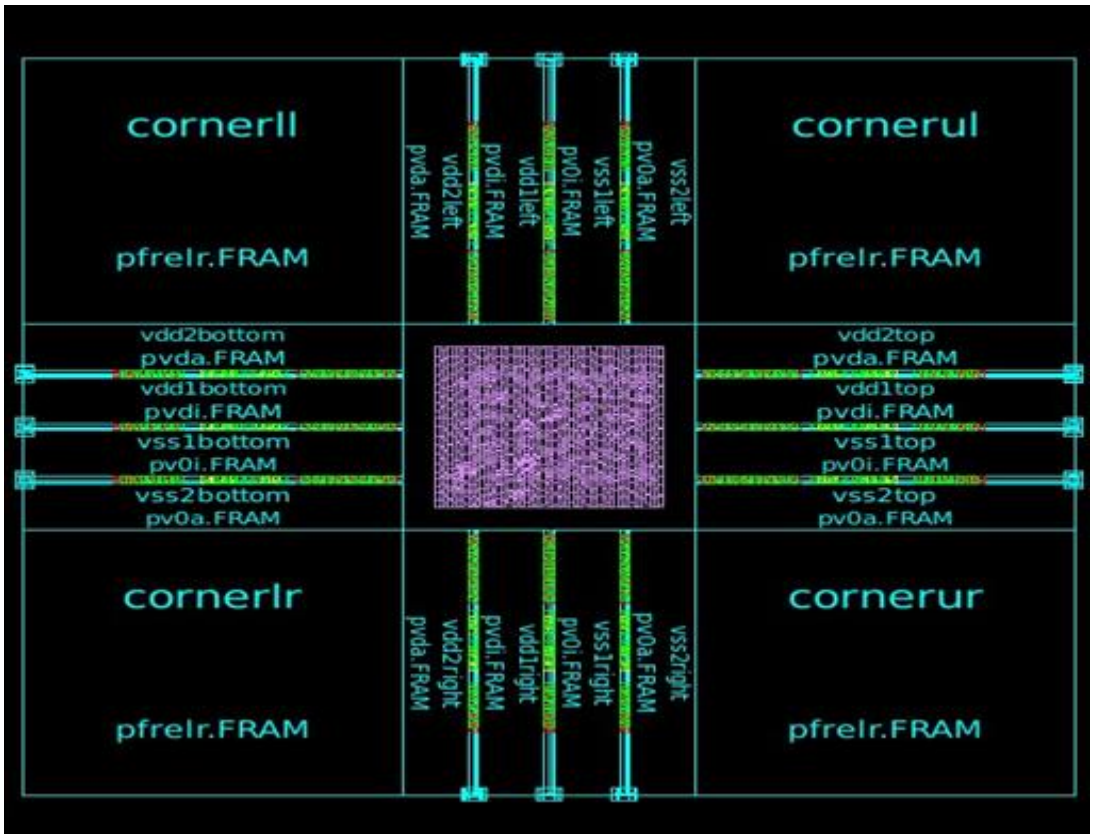

Figure 4: Layout after process placement of standard cells

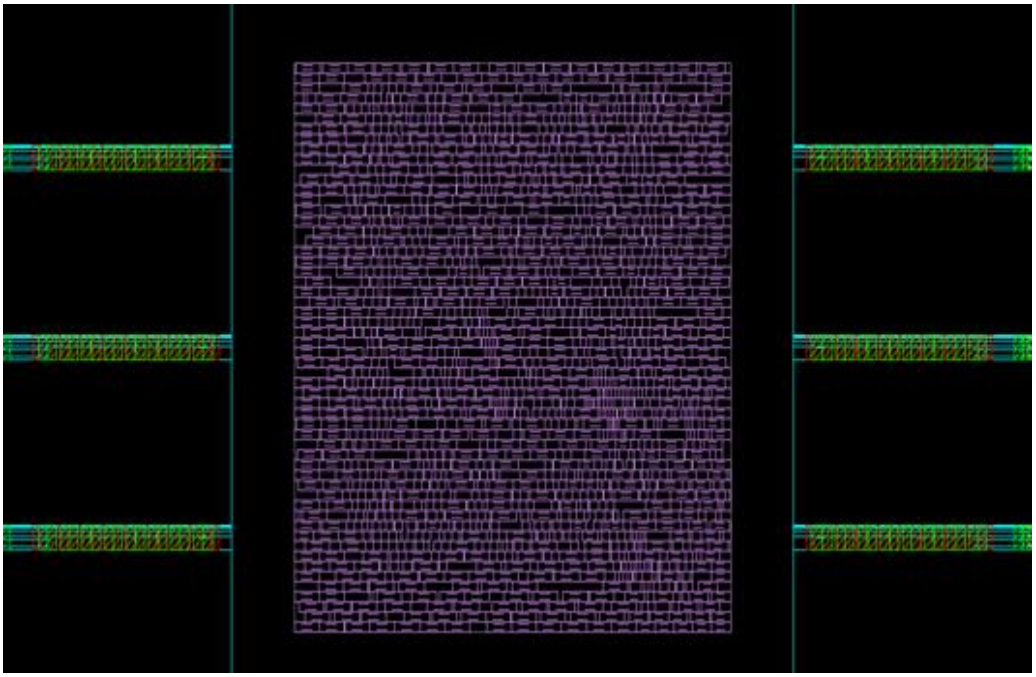

Figure 5: Layout for placed standard cells

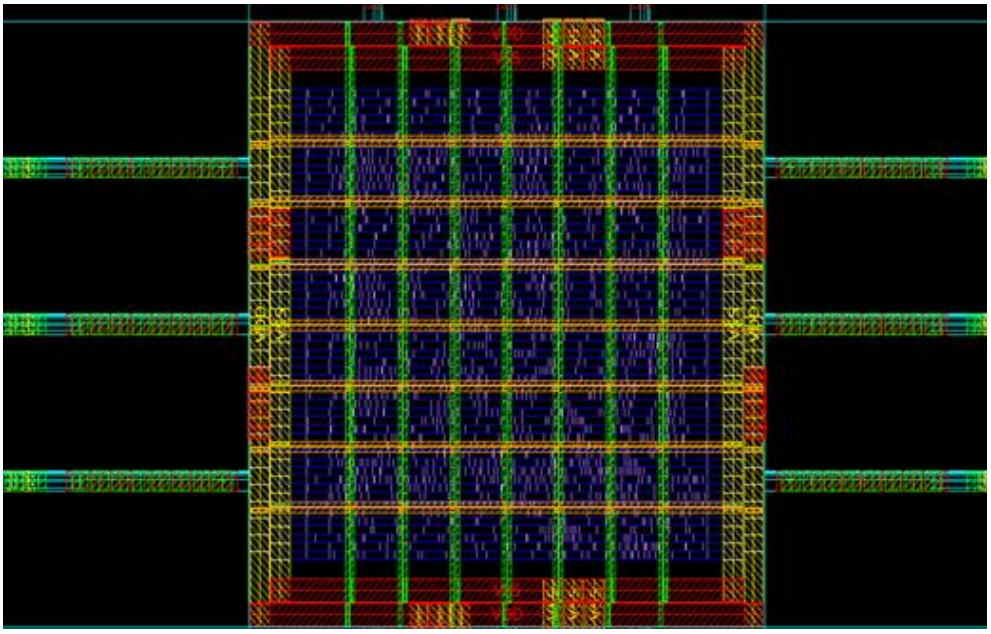

Figure 6: Layout after placement and power optimization

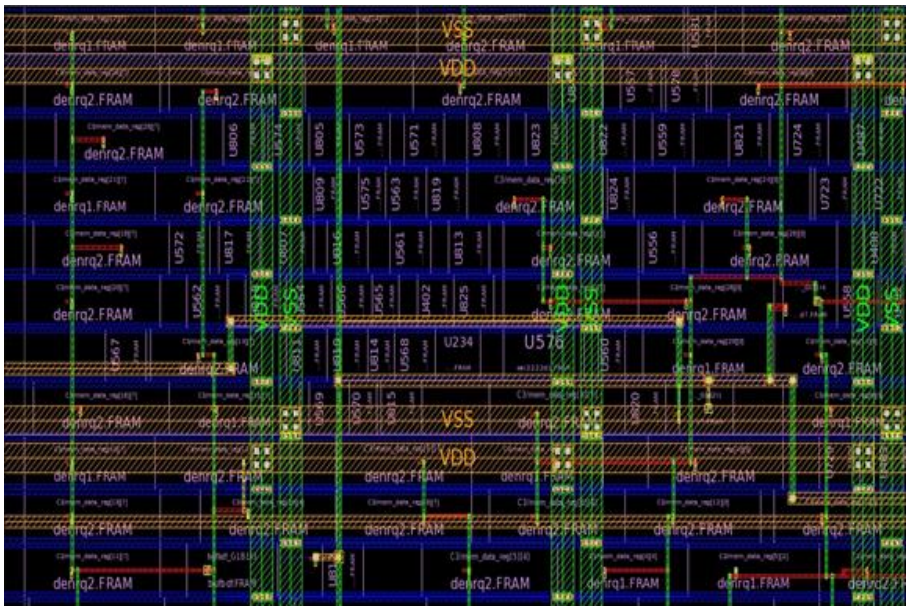

Figure 7: Layout after clock tree synthesis

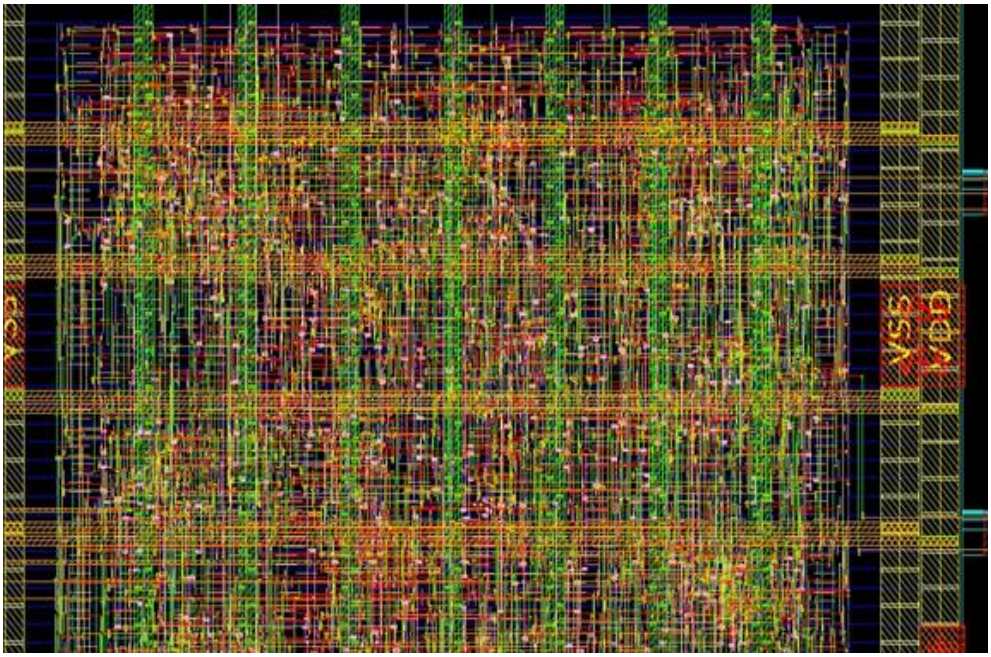

Figure 8: Layout shows routing of the design

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