

## Smart Car Parking System on FPGA For Time Efficient

Sharma Kumar Kasivishva Nathan<sup>1</sup>, Nabihah Ahmad<sup>1\*</sup>,

<sup>1</sup>Faculty of Electrical and Electronic Engineering,  
Universiti Tun Hussein Onn Malaysia, Parit Raja, 86400, Johor, MALAYSIA

\*Corresponding Author Designation

DOI: <https://doi.org/10.30880/eeee.2023.04.01.058>

Received 17 January 2023; Accepted 06 March 2023; Available online 30 April 2023

**Abstract:** This project is a smart parking system that uses infrared sensors and a Field Programmable Gate Array (FPGA) to improve the efficiency and convenience of finding parking in urban areas. The system uses a network of sensors to detect the presence of vehicles in a parking garage and LED lights to show parking space availability. The FPGA processes the sensor data in real-time and executes parking algorithms for fast and accurate results. The parking system was tested by simulating and by setting up a prototype and showed promising results with a high success rate in detecting parking spaces. The use of IR sensors and LED lights make for a cost-effective and energy-efficient design. The FPGA technology allows for flexibility and scalability, making it well-suited for use in smart parking systems. The prototype represents a small-scale implementation of the system, showcasing two levels of parking, each with four parking spaces. The LED lights indicate available parking spaces, and a display shows the total number of occupied spaces. This prototype represents a proof of concept and can be developed further for large-scale implementations. The smart parking system has the potential to significantly improve the efficiency and convenience of parking in urban areas. The prototype is checked and tested by using toy cars to check on the smart parking system.

**Keywords:** Smart Parking System, Cyclone II, Field Programmable Gate Array (FPGA)

### 1. Introduction

Smart Parking System is a solution that includes barrier gates, access control system, and smart parking system to make parking in public or private building more efficient. A conventional parking system is a type of smart parking system in a multi-level parking structure [1]. The system uses mechanical lifts, pallets, and conveyors to move vehicles between the entrance and parking spaces. With the use of vehicle detecting sensors system, car drivers can easily identify and obtain an empty parking place at any convenient car park [2]. Smart parking systems can help reduce the number of cars looking for parking, thus reducing traffic congestion and emissions. Additionally, they can improve

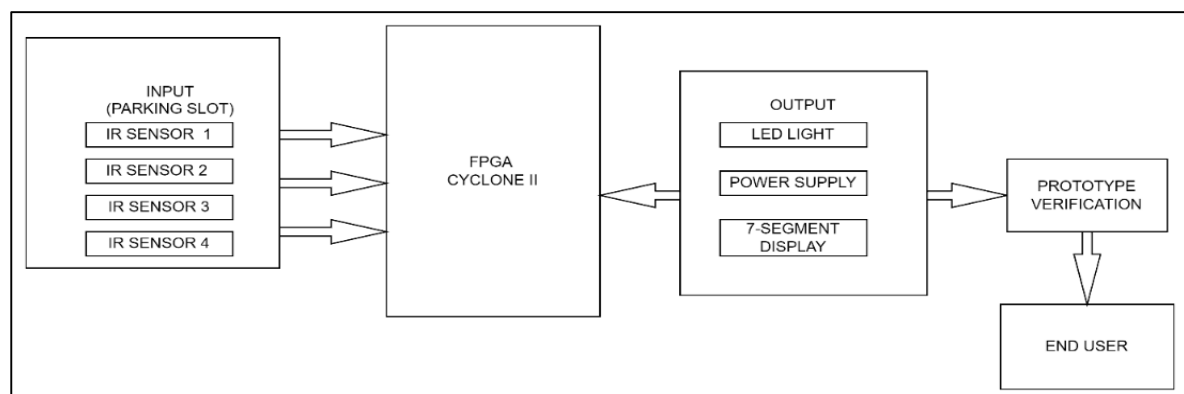
business by increasing revenue and customer satisfaction [3]. This is beneficial in regions where space is scarce, as it maximizes the use of limited space [4].

The smart parking system using Field Programmable Gate Array (FPGA) is implemented to provide a fast and smart idea for parking terms. This project is a smart parking system that uses infrared sensors and a FPGA to improve the efficiency in urban areas. The system uses infrared sensors to detect obstacles and prevent mishaps [5]. Smart parking systems designed to be a safe and efficient solution for cars, saving time, money, and space [6]. In this project, there are four main hardware which are used to complete the prototype of the smart parking system. The hardware used are the infrared sensor, led green and red, seven segment display and the FPGA board used for simulating the hardware and software.

## 2. Materials and Methods

### 2.1 Block Diagram

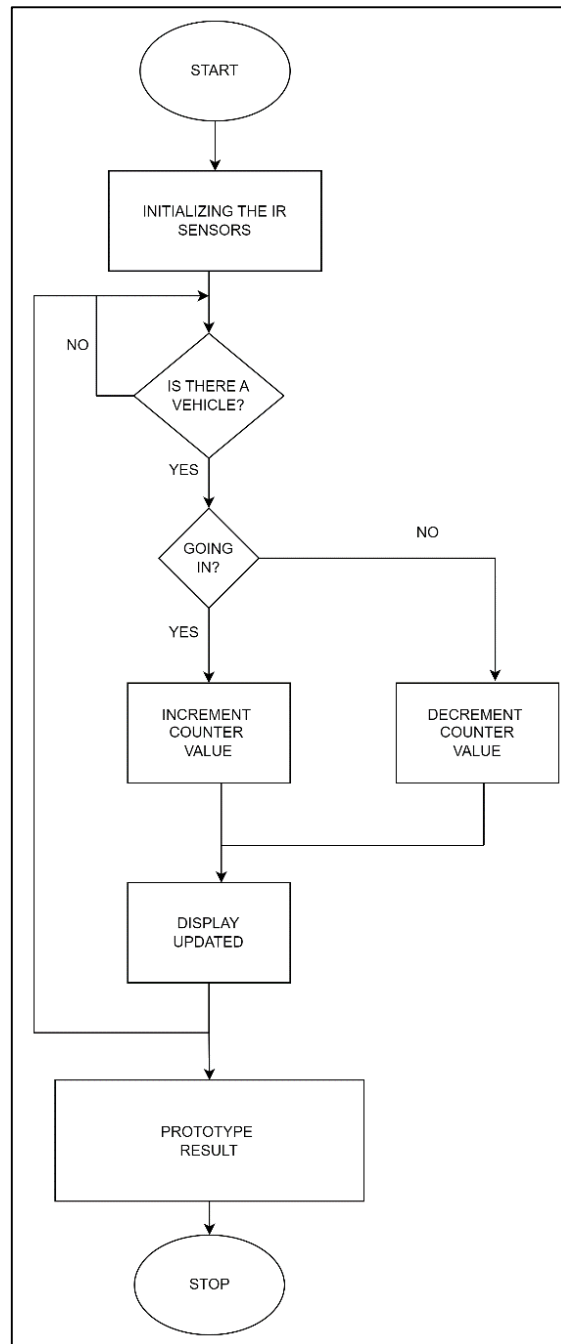
The block diagram illustrates the interaction between the Field Programmable Gate Array (FPGA) and the smart car parking system. The FPGA receives input from the infrared sensors in the parking slots and uses this information to control the LED lights, power supply, and LCD display. The FPGA, specifically the Cyclone II, is used to process the sensor data in real-time and execute the parking algorithms to provide an accurate and fast parking process [7]. After the software and hardware are assembled, the prototype verification process is performed to ensure that the smart car parking system is functioning correctly. The output of the system is also visible through a mobile application. Figure 1 shows the block diagram of the smart parking system.



**Figure 1: Block diagram of the smart parking system**

### 2.2 Methods

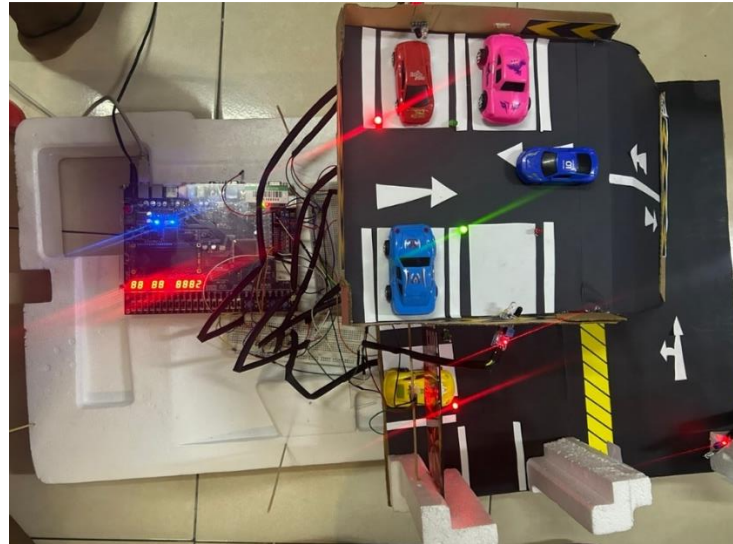
The research process began with identifying the issue and conducting a literature review to gather information on the topic [8]. Then, project objectives, scope, and methodology were established. The development process for the project followed common steps such as creating the system specification, designing the system using Verilog code, and configuring the tools for simulation and synthesis. The schematic and Verilog code were written for simulation, which was then followed by synthesis of the HDL code and post-synthesis simulation. The final step was the configuration of the FPGA for successful simulation. The smart parking system uses infrared (IR) sensors to detect when a vehicle enters or exits a parking space. The sensors send a signal to the system indicating whether a vehicle is present or not. If a vehicle is detected, the system increments the number of occupied spaces. If a vehicle is not detected, the system decrements the number of occupied spaces. The number of occupied spaces is displayed on a 7-segment display that is connected to the system. The system also updates the number of available parking spaces in the parking lot, and this information can be accessed through an application to help save time for drivers looking for a parking space. Figure 2 shows the project flow.



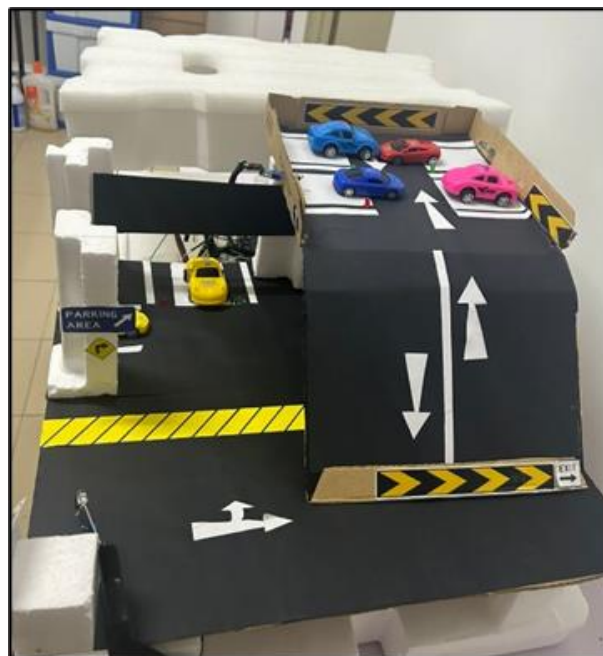
**Figure 2: The process flow**

### 2.3 Hardware Setup

The connection of the three sensors will be discussed which infrared sensor, DE 2 SOC is the main component of the project [9]. For this project, Node MCU ESP32 board, pH, temperature, and turbidity are required to be powered by 5 V by two 3.7 V 18650 lithium-ion batteries arranged in series via a DC Power Jack. The two-lithium battery will be charged by the TP4056 Type-C charger which is connected to the mini solar panel so the battery can be charged in two ways which by solar panel and Type-C port and the voltage value will be displayed in the 7-Seg Voltage Display. Figure 3 shows Circuit design of the project and Figure 4 shows the power supply circuit of the project.



**Figure 3: Circuit design**



**Figure 4: Circuit prototype**

### **3. Results and Discussion**

#### **3.1 Software result and setup**

A smart parking system RTL viewer in Quartus is a tool that allows developers to view and debug the design of a smart parking system using a graphical interface. It displays the design at the level of digital logic gates and flip-flops, helping developers to troubleshoot and debug the system. The RTL viewer can monitor the status of components such as LED, 7-segment, Clk, rst and sensors in real-time, allowing developers to identify and fix any issues. Additionally, it enables developers to optimize the performance of the design by fine-tuning the timing and resource usage of the system. It helps developers to identify problems and fix them easily, making the system more reliable and efficient. Figure 5 shows the RTL viewer of the smart parking system.

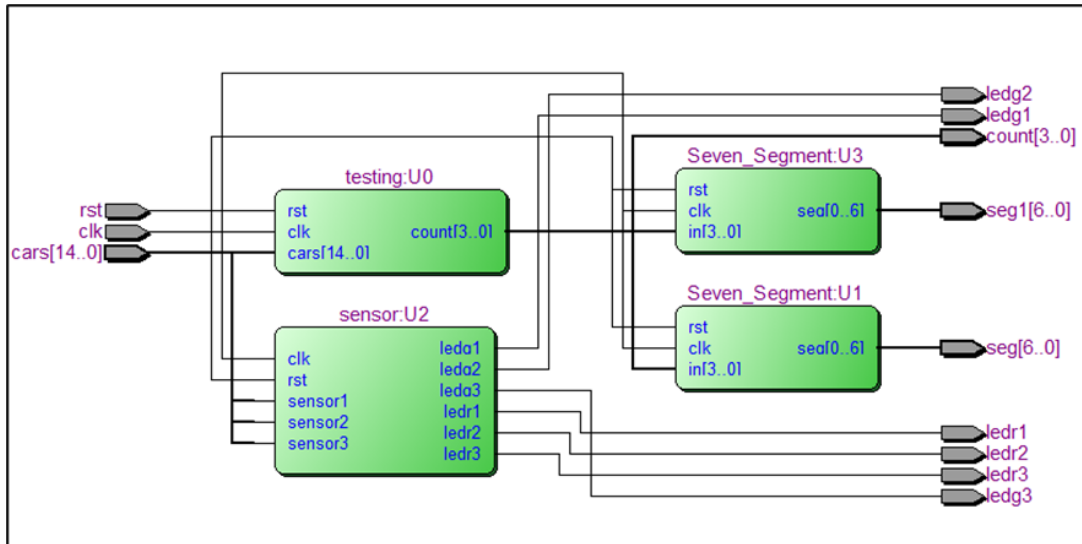


Figure 5: RTL Viewer

### 3.2 Test result of software

The System Verification Report for a Smart Parking System would provide an overview of the system, including the use of FPGA, IR sensors, LED lights, and counter. It would detail the testing and verification methods used, including testbenches and simulations, and provide results from those tests including any bugs found and resolved, performance data and charts. The report would also include recommendations for further development or improvement and list references used. Additionally, the report would have an appendix for any additional supporting materials such as source codes and schematics. The report would be a comprehensive documentation of the system's functionality and performance, and any issues found and resolved during the verification process. Figure 6 shows the report of system verification.

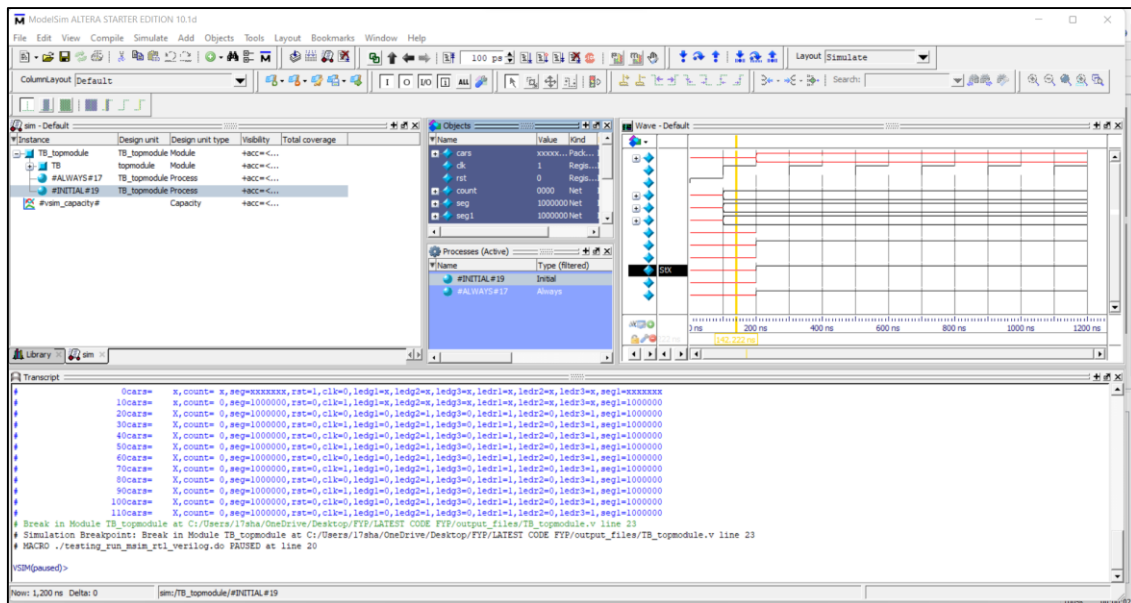


Figure 6: Report of system verification

### 3.3 System verification

The testbench for a smart parking system module verifies its functionality by instantiating the module and connecting it to inputs such as `cars`, `rst`, and `clk`, and outputs such as `count`, `seg`, `ledg1`, `ledg2`, `ledg3`, `ledr1`, `ledr2`, `ledr3`, and `seg1`. It also sets up a monitoring system that continuously displays

the values of the inputs and outputs. The testbench also includes an initial block of code that creates a clock signal with a period of 10 ns and sets the reset signal to be active initially. It also sets the value of cars to 100 after 10 ns and stops running after 100 ns. A timescale of 10ns/1ns is also included at the top to indicate the time unit for the # and `` operators. The output of the timing diagram shows how the led and counter initiate. Figure 7 shows system verification.

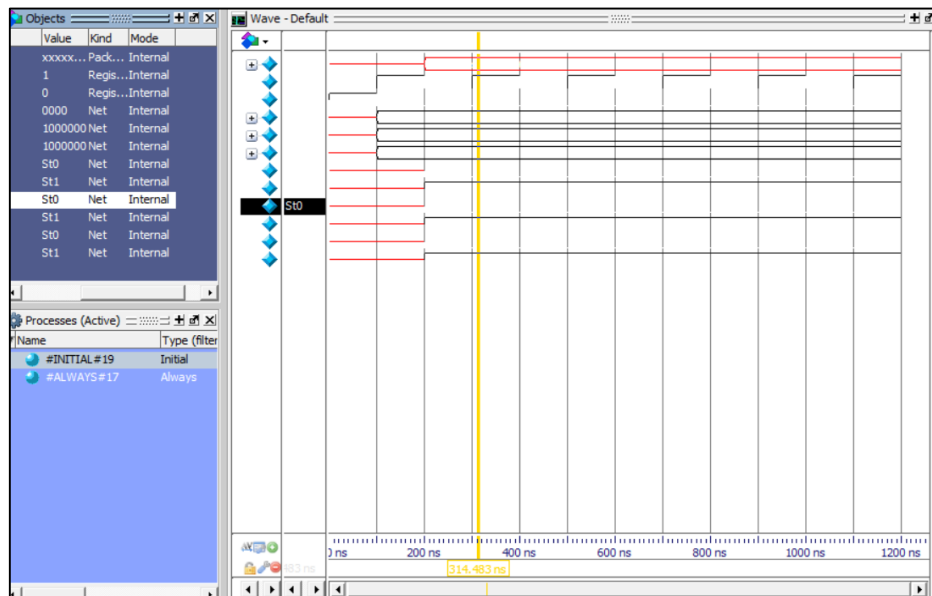


Figure 7: System verification

#### 4. Conclusion

In conclusion, designing a smart parking system using FPGA technology is a highly efficient and effective way of managing parking. The use of FPGA allows for a flexible and adaptable system that can be easily upgraded to meet the changing needs of the parking industry. With its high-speed and high-precision processing capabilities, the system can achieve a high degree of accuracy and reliability. A prototype of this system can be a valuable step in testing and evaluating the proposed system and its features. By implementing the prototype in a real-world setting, feedback can be gathered from users and used to improve the system's usability and user-friendliness. Additionally, it can help to reduce traffic congestion, increase customer satisfaction, and boost revenue for the mall. Verifying a prototype of a smart parking system is crucial to ensure its functionality and effectiveness and identify any scalability issues that may arise.

#### Acknowledgement

The authors would also like to thank the Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia for its support.

#### References

- [1] P. Wessel, "What is Smart Parking? | Parksmart," Jan. 07, 2016. <https://parksmart.gbci.org/what-smart-parking> (accessed Jun. 16, 2022).
- [2] Devi, S. S., JJR, B. A., & AI, K. (2020). Car Parking System Using FPGA. *International Research Journal on Advanced Science Hub*, 2(8), 88-93.
- [3] Rupali Bharwaj, Menika Seth, Kawaljit Singh Dhudike, "Use of Automation of Machines and Control System to Optimize Car Parking using Embedded Approach" *International Journal*

Advanced Research in Computer Science and Software Engineering, Volume 4 Issue 6 June 2014, pp.686-691.

- [4] M. Nasreen, M. Iyer, E. P. Jayakumar, and T. S. Bindiya, "Automobile Safety and Automatic Parking System using Sensors and Conventional Wireless Networks," 2018 IEEE 3rd International Conference on Computing, Communication and Security (ICCCS), 2018, pp. 51-55, doi: 10.1109/CCCS.2018.8586833.
- [5] S. N. Shinde and S. S. Chorage, "Intelligent car parking system," 2016 International Conference on Inventive Computation Technologies (ICICT), 2016, pp. 1-4, doi: 10.1109/INVENTIVE.2016.7830244.
- [6] M. N. S. Shahi, S. S. Muhaimin, M. M. Nishat, F. Faisal and M. S. B. Motahar, "Automated Vehicle Access and Exit Control: A Smart Parking Management System using Finite State Machine in VHDL," 2022 Research, Invention, and Innovation Congress: Innovative Electricals and Electronics (RI2C), Bangkok, Thailand, 2022, pp. 170-177, doi: 10.1109/RI2C56397.2022.9910305.
- [7] Amin, Ahmad Fairuz Muhd, et al. "Embedded System Implementation on FPGA System With  $\mu$ CLinux OS." IOP Conference Series: Materials Science and Engineering. Vol. 17. No. 1. IOP Publishing, 2011.
- [8] Kaur, Ramneet, and Balwinder Singh. "Design and implementation of car parking system on FPGA." arXiv preprint arXiv:1307.3051 (2013).
- [9] Obaid, Zeyad Assi, Nasri Sulaiman, and M. N. Hamidon. "FPGA-based implementation of digital logic design using Altera DE2 board." International journal of computer science and network security 9.8 (2009): 186-194.