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Analysis of Symmetric and Asymmetric Multilevel Inverter Topologies with Focus on THD Performance

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Abstract

Inverters are important components in modern power conversion systems, including renewable energy applications and electric vehicles, where the conversion of DC power to high-quality AC output is essential. With the growing demand for power quality, minimizing Total Harmonic Distortion (THD) is crucial, as high levels can degrade system performance and cause equipment failure. This project aims to simulate and compare symmetric and asymmetric cascaded H-bridge (CHB) multilevel inverters to determine the most efficient topology for power electronics applications. The study involves developing separate PLECS models for a 5-level symmetric and a 7-level asymmetric CHB inverter, implementing Sinusoidal Pulse Width Modulation (SPWM) and Level-Shifted SPWM (LSSPWM), respectively, and applying an LCL filter to the output of each. The results show that the unfiltered THD for the symmetrical 5-level inverter was 27.00%, which was reduced to 0.13% after LCL filtering. The asymmetrical 7-level inverter inherently performed better, with an initial THD of 17.42% that improved to 4.38% after filtering. These findings conclude that both inverter designs, particularly the asymmetric topology with their finer voltage steps, effectively meet harmonic standards below the required 5% threshold after filtering, validating their suitability for real-world systems.

1. Introduction

Inverters are important for power conversion systems as components in renewable energy applications, uninterruptible power supplies (UPS), electric vehicles (EVs), and industrial motor drives by converting DC power into high-quality AC output. With increasing demand for energy efficiency and power quality, minimizing Total Harmonic Distortion (THD) has become crucial, as high THD can lead to reduced system performance, overheating, and equipment failure. Multilevel inverters (MLIs), especially symmetric and asymmetric cascaded H-bridge topologies, have gained attention due to their ability to generate near-sinusoidal waveforms with lower harmonic content and higher efficiency compared to conventional two-level inverters. Previous studies have shown that asymmetric CHB inverters, using unequal DC sources, can achieve better THD performance and require fewer components than symmetric designs, although they involve more complex control strategies [1]-[3].

This project aims to simulate and compare both symmetric and asymmetric CHB multilevel inverters using PLECS, implementing Sinusoidal Pulse Width Modulation (SPWM) and LCL filtering, with a focus on analyzing and reducing THD before and after filtering to determine the most efficient and practical topology for power electronics applications.

2. Design and Calculation Analysis

2.1 LCL Filter Design Analysis

An LCL filter was chosen to produce a smooth sinusoidal output with low harmonic distortion. It includes two inductors—one on the inverter side and one on the grid or load side—and a capacitor in between. This setup reduces high-frequency harmonics more effectively than a basic LC filter due to its sharper filtering ability. LCL filters are a good match for multilevel inverters, which often run at lower switching frequencies. They can reduce harmonics without needing large components. The filter was designed to avoid resonance near the 50 Hz fundamental frequency and to keep performance stable. The values of the inductors and capacitors were chosen to reduce current ripple, control reactive power, and limit resonance. The LCL filter improves the output quality of multilevel inverters and supports compliance with harmonic standards in systems like renewable energy and industry.

2.2 LCL Filter and THD Calculation

The goal of the LCL filter design is to select appropriate values for the inverter-side inductor (L1), the grid-side inductor (L2), and the capacitor (C or C1) to effectively filter switching harmonics with minimal power loss. First, to find a nominal AC current that the inverter will produce, Eq. (1) is used.

$$Irated = \frac{Prated}{(Vrated \times PF)} \tag{1}$$

where $Irated$ is the rated RMS (root mean square) output current in Amperes (A), $Prated$ is the inverter's rated active power in Watts (W), and $Vrated$ is the rated RMS grid voltage in Volts (V). For a three-phase system, this is the line-to-neutral voltage. While PF is a power factor. For grid-tied inverters, this is usually assumed to be 1.

Inverter-side inductor's (L1) in Eq. (2) primary job is to limit the current ripple caused by the inverter's high-frequency switching. A common design practice is to allow a peak-to-peak ripple current that is 10-25% of the rated peak current.

$$L1 \approx \frac{Vdc}{4 \cdot fsw \cdot \Delta iL, max} \tag{2}$$

where Vdc is DC voltage input to the inverter. The fsw is an inverter's switching frequency (e.g., 10 kHz, 20 kHz) and $\Delta iL, max$ is the maximum desired peak-to-peak current ripple. Grid-side inductor works to attenuate the harmonics further. Using $L1$=$L2$ is a common simplification that creates a symmetrical filter, which can simplify the design. However, L2 can also be designed as a fraction of $L1$ (e.g., $L2$=0.5·L1) depending on the specific filtering requirements.

Filter capacitors (C or C1) shunt the high frequency harmonics to the ground. The standard method is to size the capacitor based on the amount of reactive power it consumes. This is typically limited to less than 5% of the inverter's rated power to avoid impacting the system's power factor. The standard equation for a capacitor in Eq. (3).

$$C = k \cdot \frac{Prated}{2\pi fg \cdot (Vrated^2)} \tag{3}$$

where C is the capacitance in Farads (F) and k is the fraction of reactive power allowed. A typical value is 0.05 (for 5%). $Prated$ is the inverter's rated power in Watts (W) and fg is the grid frequency (e.g. 50 Hz or 60 Hz). Lastly is $Vrated$, the rated RMS grid voltage in Volts (V).

After selecting $L1$, $L2$, and C, you must check the filter's resonant frequency ($fres$) in Eq. (4) to ensure it does not cause instability. It should be well above the grid frequency but below the switching frequency.

$$fres = \left(\frac{1}{2\pi}\right)\sqrt{\frac{L1 + L2}{C * L1 * L2}} \tag{4}$$

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Lastly, the THD is calculated in Eq. (5). THD measures the level of distortion in the output current, or voltage waveform compared to an ideal sine wave.

$$THD = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \cdots V_n{}^2}}{V_1} * 100 \quad (5)$$

2.3 Methodology

In modelling of multilevel inverters, we have developed separate PLECS models for both Symmetrical and Asymmetrical Multilevel Inverter circuits, focusing on how their design principles and modulation strategies impact their performance and the number of output voltage levels.

2.3.1 Symmetrical Multilevel Inverter and Asymmetrical Multilevel Inverter

In the symmetrical multilevel inverter (SMLI) model, each H-bridge (or cascade cell) utilizes identical DC sources. This means that the voltage supplied to all DC sources within the topology is the same. For SMLI using two DC sources, the model specifies two DC voltage sources, each at 170V, and a total of eight switches. Generally, in symmetrical topologies, the number of output voltage levels is determined by the formula *Nlevel = 2n + 1*, where *n* is the number of DC sources. For a symmetrical model with *n = 2 DC* sources, this results in *2X2 + 1 = 5* output voltage levels. The number of switches used is typically 4n, which in your case would be *4X2 = 8* switches. This configuration is common for cascaded H-bridge topologies, where each H-bridge can generate three voltage levels *(+Vdc, 0, -Vdc*).

The AMLI uses unequal DC sources, which allows for generating higher voltage levels with fewer cells. Asymmetrical feeding, where partial cells are supplied with unequal DC voltages, increases the number of levels in the generated output voltage without adding complexity or increasing components to the existing topology. With two H-bridges and unequal DC sources, an AMLI can typically achieve 7 voltage levels. Some asymmetrical topologies with two H-bridges can even achieve 9 voltage levels with ternary progression ratios (1:3:9) [4][5]. A particular proposed 7-level asymmetrical MLI topology requires only six switches and two voltage sources.

2.3.2 Switching Strategy for Asymmetric and Symmetric

Both asymmetrical and symmetrical multilevel inverters (MLIs) widely utilize SPWM techniques. SPWM is a general approach that involves comparing a sinusoidal reference waveform with triangular carrier waveforms to generate the necessary switching signals for the inverter's power devices. An Asymmetrical circuit uses the Level-Shifted SPWM technique, while a Symmetric circuit uses the SPWM technique. For asymmetrical multilevel inverters (AMLIs), which are characterized by their use of unequal DC voltage sources, specific multi-carrier Level-Shifted PWM techniques are commonly applied. These variations are designed to effectively manage the differing DC source magnitudes and maximize the number of output voltage levels.

2.3.3 Level-Shifted SPWM for Asymmetric Switching Technique

In LSPWM for multilevel inverters, these six triangular carrier signals are vertically shifted and usually placed in continuous bands around the zero reference [6]. Fig. 1 illustrates the gate pulse waveform of the Asymmetrical circuit.

The operation is split into two halves, one for positive voltages and one for negative voltages, likely controlling the two separate H-bridges of the inverter. Positive Level Generation (Left Side): The sine wave is compared to the three carriers that occupy the positive voltage levels ([0V to 1V], [1V to 2V], and [2V to 3V]). The relational operators (comparators) and logic gates (XOR, NOT) process these comparisons to generate the switching signals A, B, C, and D. Negative Level Generation (Right Side): In parallel, the same sine wave is compared to the three carriers in the negative voltage range ([-1V to 0V], [-2V to -1V], and [-3V to -2V]). A similar set of logic gates creates the switching signals E, F, G, and H.

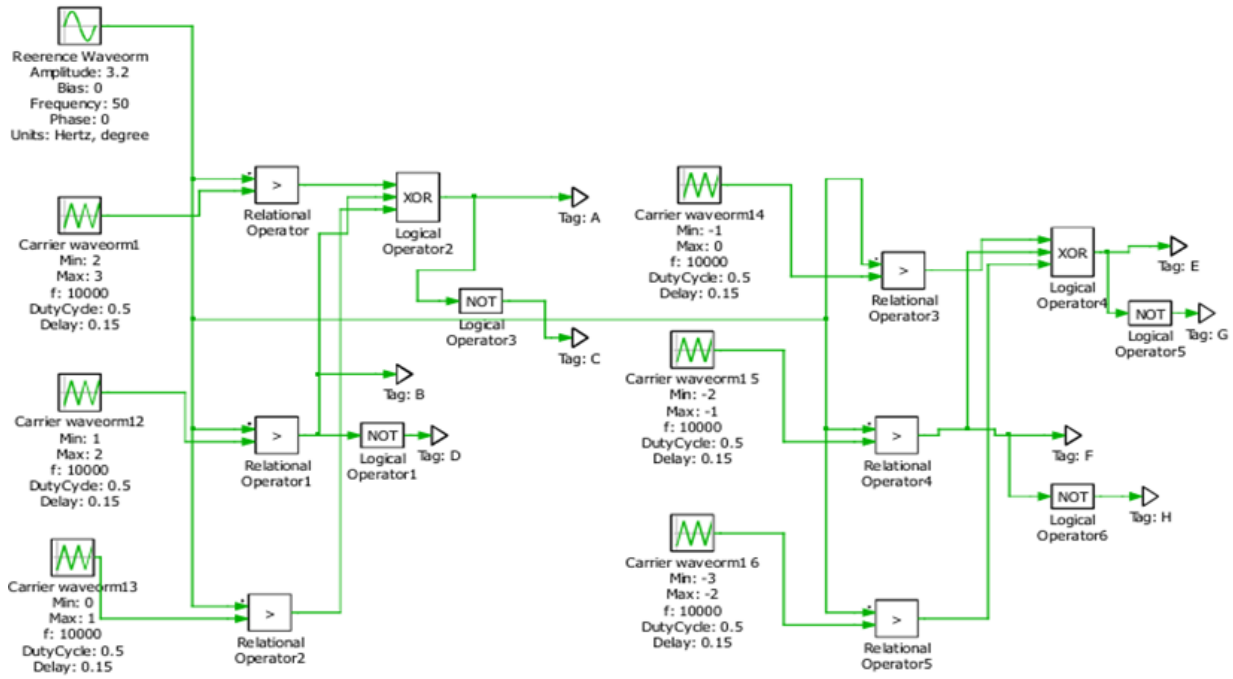

Fig. 1 *Diagram of LS-SPWM*

2.3.4 Sine Wave PWM for Symmetric Circuit

SPWM, also known as multi-carrier Pulse Width Modulation (PWM) or Carrier Switching Frequency Sub Harmonic Pulse Width Modulation (CSFSHPWM), is a widely used control technique for inverters. Fig. 2 shows the SPWM circuit or symmetric [7].

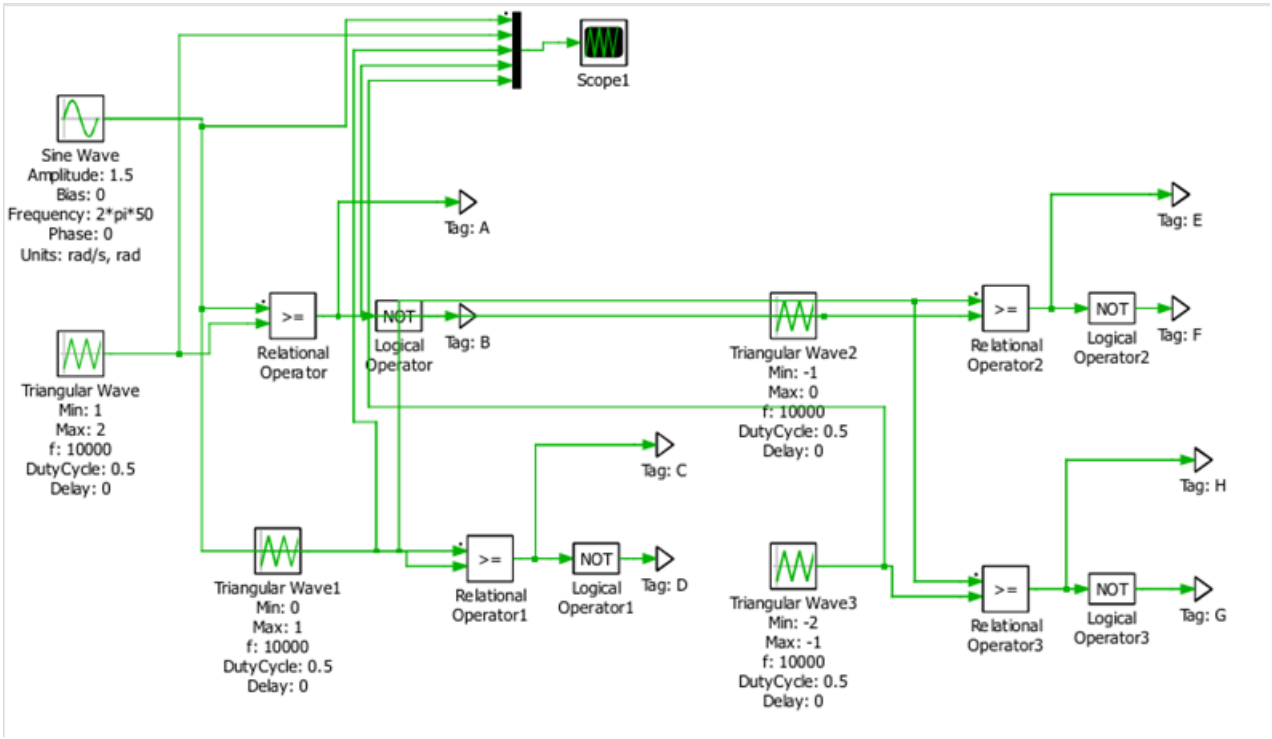

Fig. 2 *SPWM circuit or symmetric*

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This circuit generates eight digital PWM signals (A to H) to control a five-level cascaded H-bridge inverter using SPWM. It works by comparing a 50 Hz sine wave (reference signal) with four high-frequency triangular carriers (10 kHz), each placed at a different vertical level. The sine wave has a peak of 2, which sets the inverter output range to −2, −1, 0, +1, and +2. Each of the four triangular carriers is compared with the sine wave using a relational operator (comparator). If the sine is greater than the carrier, the output is logic high (1); otherwise, it is low (0). Each comparison produces two opposite signals: one from the comparator (e.g., signal A), and its inverted version using a NOT gate (signal B). This is repeated to get four pairs: (A, B), (C, D), (E, F), and (G, H).

2.3.5 Cascaded H-Bridge or Symmetrical and Asymmetrical

In a symmetric topology, all DC voltage sources supplying the H-bridge cells have equal magnitudes. For example, a 7-level symmetric inverter might use three equal DC sources, each contributing a voltage 'V', to achieve levels like +3V, +2V, +V, 0, -V, -2V, and -3V. Output Voltage Levels: The number of output voltage levels (N) for a symmetric CHB MLI with DC sources is typically determined by the formula N = 2n + 1. For instance, a 7-level symmetric CHB inverter requires three H-bridge cells. In an asymmetric topology, the H-bridge cells are supplied by DC voltage sources of unequal magnitudes [8]. The ratio of these DC sources often follows a binary progression or sometimes a trinary progression. For example, a 7-level asymmetrical inverter might use two DC voltage sources in a 1:2 ratio (e.g., Vdc and 2Vdc) or 1:3 ratio [10]. A 15-level asymmetric inverter could use sources in a 1:2:4 ratio. The proposed circuit for both topologies uses the same amount of input voltage and MOSFET for accurate comparison analysis. Fig. 3 shows the proposed cascaded circuit[8][9][10].

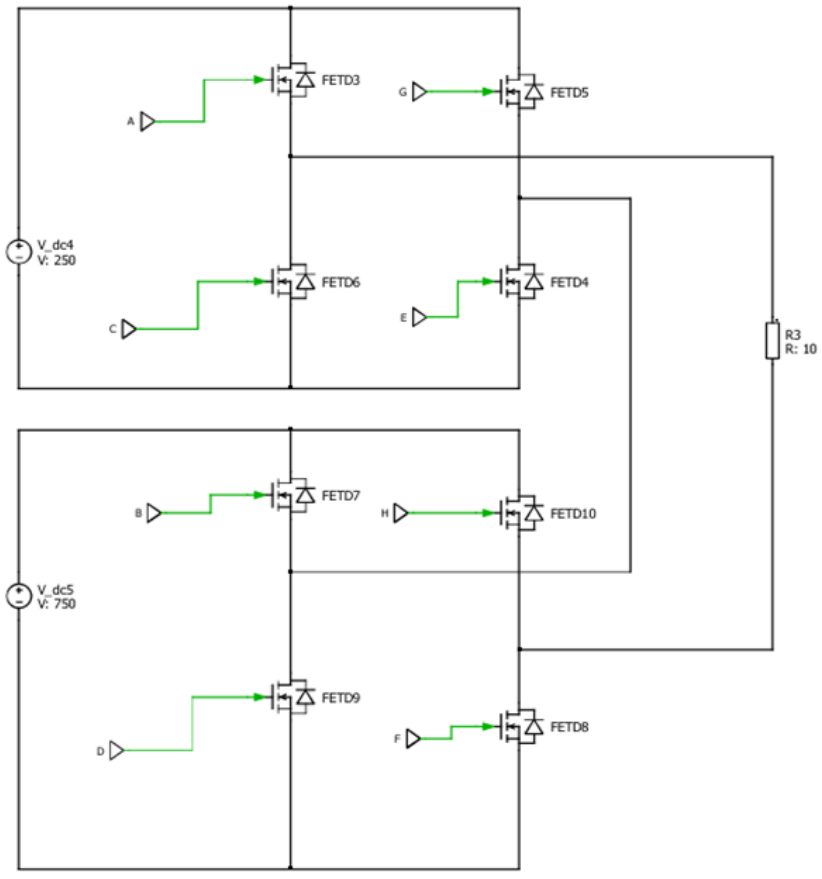

Fig. 3 *Proposed cascaded circuit*

3. Results and Discussion

This section presents the simulation results for both the symmetrical 5-level cascaded H-bridge (CHB) and the asymmetrical 7-level CHB inverter topologies. Results focus on output voltage and current waveforms, harmonic analysis, and the effects of LC filtering.

3.1 Voltage and Current Waveforms Before and After Filtering

Fig. 4 and 5 illustrate the simulated output voltage and current waveforms of the symmetrical 5-level inverter before and after LCL filtering. Before filtering, the voltage waveform exhibits clear stepped levels corresponding to the switching states. After applying the LCL filter, the waveform is noticeably smoothed, approaching a near-sinusoidal shape with reduced ripple.

Additionally, the voltage and current waveforms of the asymmetrical 7-level CHB inverter are displayed in Fig. 6 and 7. The unfiltered waveform already exhibits a closer resemblance to a sinusoidal shape due to the increased number of levels, and the output is even higher quality with less distortion after filtering.

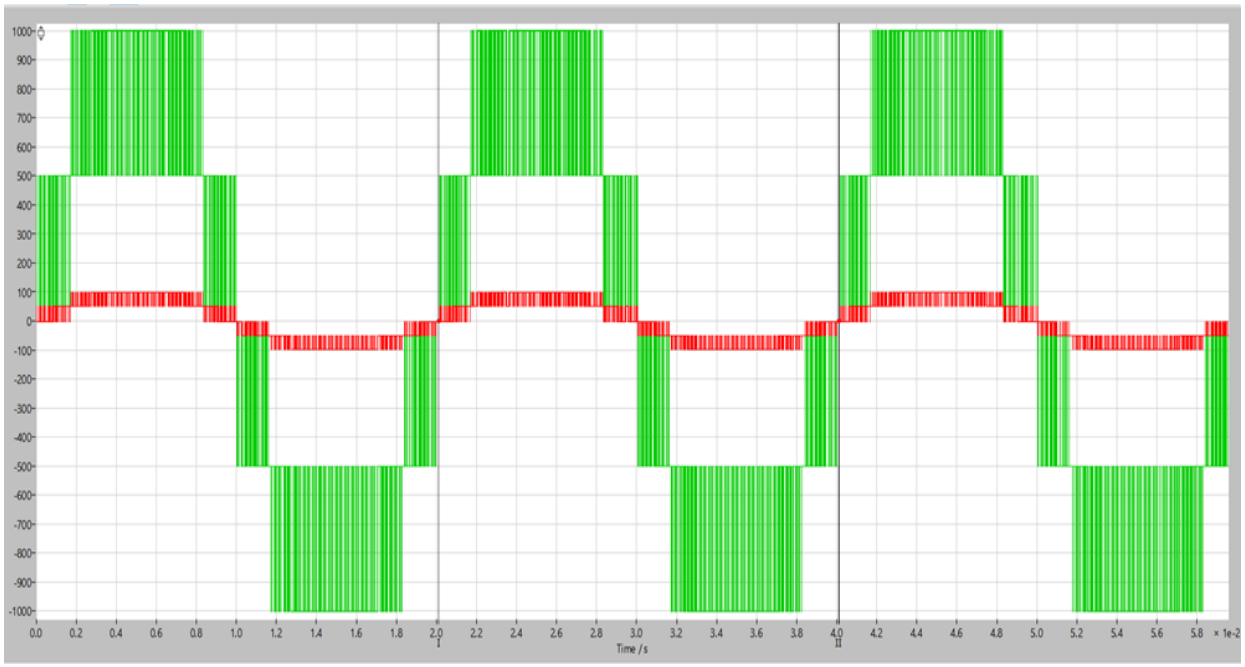

Fig. 4 *Symmetrical 5-level inverter before LCL filtering*

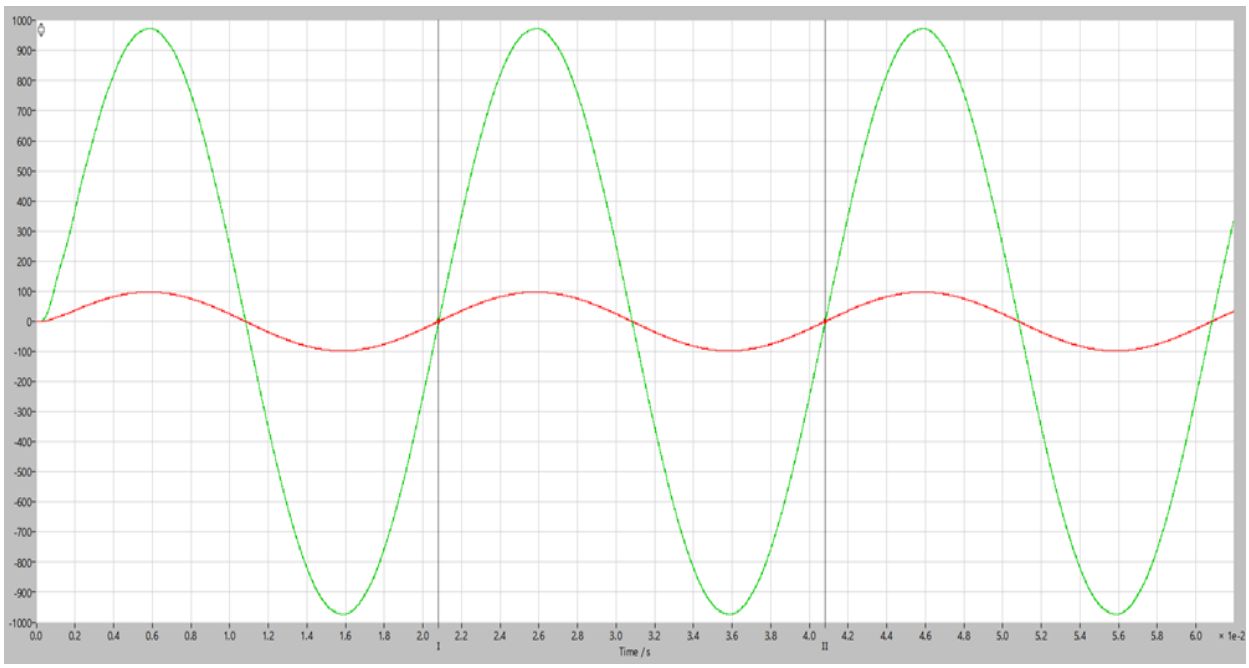

Fig. 5 *Symmetrical 5-level inverter after LCL filtering*

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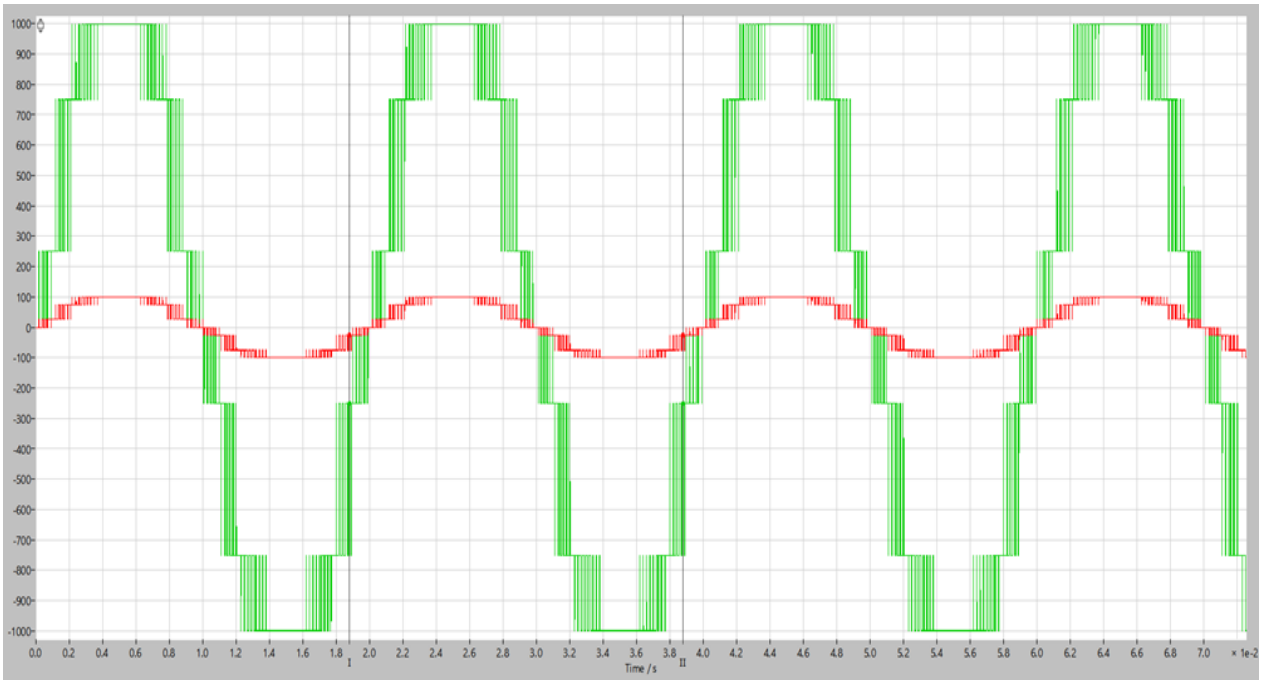

Fig. 6 *Asymmetrical 7-level inverter before LCL filtering*

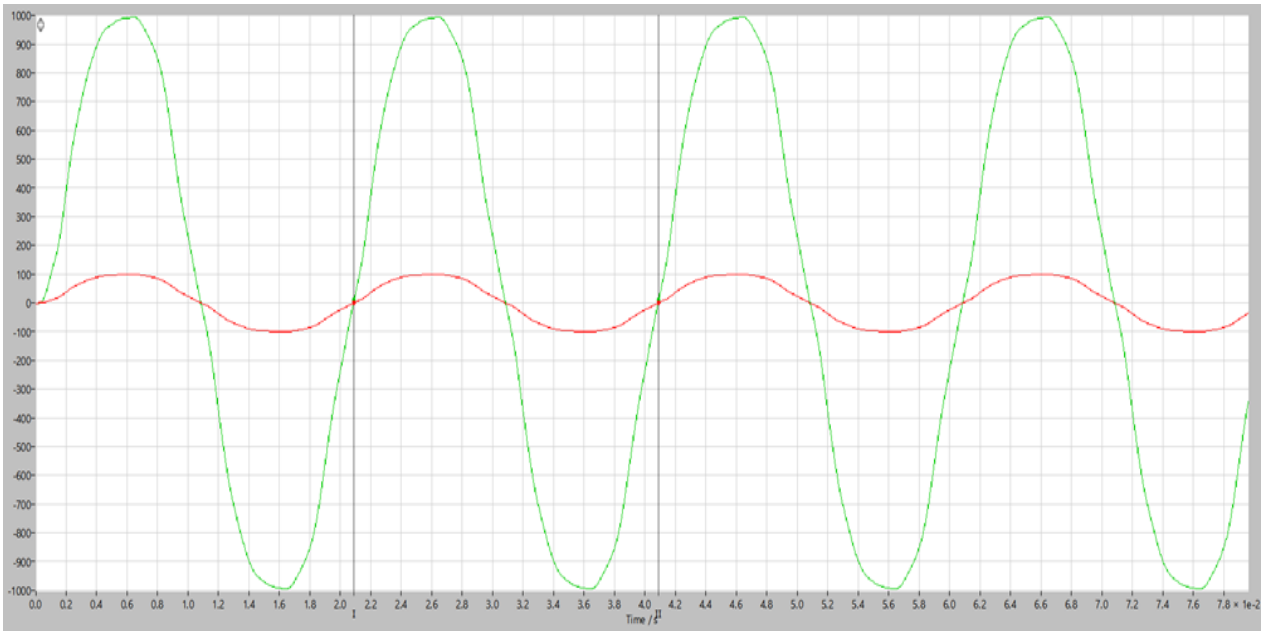

Fig. 7 *Asymmetrical 7-level inverter after LCL filtering*

3.2 FFT Analysis and THD Comparison (Before vs. After Filtering)

FFT analysis was performed on the output voltage of both inverter topologies to quantify their harmonic content. For the symmetrical 5-level CHB inverter, the THD before filtering was measured at 27.00% (0.270017). After applying the LC filter, the THD was reduced drastically to 0.13% (0.00131776), demonstrating the effectiveness of the filter in suppressing harmonic components.

For the asymmetrical 7-level CHB inverter, the unfiltered THD was 17.42% (0.174234). After filtering, the THD improved to 4.38% (0.0438051). These results clearly confirm that higher-level inverters (7-level) inherently have lower harmonic distortion due to finer output steps, and the application of an LC filter significantly improves waveform quality for both topologies. Both filtered waveforms achieve THD values well below the 5%

recommended threshold set by Malaysian grid connection standards, validating the design's compliance with harmonic requirements.

3.3 Effectiveness of Filter Design in Reducing THD

An LCL filter was used to reduce harmonics more effectively than a basic LC filter. It includes two inductors and a capacitor, which together block high-frequency harmonics better because of an extra resonance point. Simulation results showed strong performance. In the symmetrical 5-level CHB inverter, total harmonic distortion (THD) dropped from 27.00% to 0.13% after filtering. In the asymmetrical 7-level CHB inverter, THD went from 17.42% to 4.38%.

The filter was tuned to avoid resonance near the switching frequency and to keep the system stable. It helped smooth the output and meet harmonic limits. Overall, the LCL filter worked well and is a good choice for multilevel inverters needing clean sinusoidal output.

4. Conclusion

Simulation and analysis of both symmetric and asymmetric cascaded H-bridge multilevel inverters (CHBMLI) showed that using an LCL filter greatly improved output quality by reducing THD to acceptable levels. The symmetric 5-level inverter achieved THD below 5%, while the asymmetric 7-level inverter performed better due to smaller voltage steps.

These results confirm that the inverters meet project goals for waveform quality, switching method, and harmonic control. Future work could improve performance further by using advanced control methods like selective harmonic elimination or space vector modulation, and by refining filter designs. These inverters are suitable for real-world use in areas such as renewable energy, electric vehicles, and grid systems where clean power and good efficiency are important.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The authors are responsible for the study conception, research design, data collection, data analysis, result interpretation and manuscript drafting.

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