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Performance Evaluation of Three-Phase Multilevel Inverter with R-Load Using SPWM

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Abstract

This project focuses on the design and performance evaluation of a three-phase symmetric multilevel inverter using Sinusoidal Pulse Width Modulation (SPWM) and an RL load. The system is developed and simulated using PLECS software with a maximum DC input of 1000 VDC and a load resistance of 10 Ω. To improve output waveform quality and meet Malaysian power standards, an LC filter is designed using a 4.7 µF capacitor and a 5.4 mH inductor, achieving a cutoff frequency of 1000 Hz. The analysis confirms that the Total Harmonic Distortion (THD) of the output voltage is reduced from approximately 68 % to below 1.5%, demonstrating the filter's effectiveness and the inverter's suitability for clean power delivery. This result confirms that the proposed design effectively meets the power quality standards with a low-distortion sinusoidal output.

1. Introduction

An inverter is a power electronic device used to convert energy from one form to another, most commonly from direct current (DC) to alternating current (AC) at a specified voltage and frequency [1]. The input can be supplied from a DC source or derived from an AC source through a rectifier, whether single-phase or three-phase. Inverters are widely used in applications such as Adjustable Speed Drives (ASD) and Uninterruptible Power Supplies (UPS) [1]. There are different types of inverters, including Voltage Source Inverters (VSI), Current Source Inverters (CSI), and Current Regulator Inverters. The quality of the inverter output is often assessed by analyzing harmonic distortion, particularly Total Harmonic Distortion (THD). Low harmonic distortion is essential for ensuring efficient power conversion, minimizing losses, and preventing performance degradation in connected equipment [2]. Excessive harmonics can lead to overheating, electromagnetic interference, and reduced lifespan of electrical devices. This study focuses on developing a simulation model of a three-phase inverter using suitable software tools, analyzing its Sinusoidal Pulse Width Modulation (SPWM) switching and the resulting waveform distortion, and evaluating the overall performance of the inverter based on THD and waveform quality.

Harmonic distortion is caused by nonlinear devices in power systems. A nonlinear device is one in which current is not proportional to applied voltage [1]. The quality of an inverter's output voltage is highly dependent on the level of total harmonic distortion. THD is a measurement that quantifies the effective value of the harmonic components present in a distorted waveform [3].

Previous studies mainly rely on ideal SPWM control without integrating a well-designed filter to address switching harmonics efficiently. To address these limitations, this study proposes a three-phase symmetric

multilevel inverter using SPWM with an optimized LC filter design to significantly reduce the THD and improve the output waveform quality. The contribution of this paper is related to the comprehensive PLECS simulation model for three-phase SPWM and performance comparison of unfiltered and filtered inverter output, highlighting the effectiveness of the filter in harmonic reduction.

2. Design and Calculation Analysis

This project employed a symmetric three-phase multilevel inverter architecture to enhance the output waveform and reduce harmonic distortion. This gadget produces stepped AC waveforms on each output phase by utilizing several identical DC sources. The inverter comprises three legs, corresponding to each phase: A, B, and C. Each leg of a full-bridge design contains two power semiconductor switches (IGBTs or MOSFETs). Anti-parallel connections link freewheeling diodes to each switch. This enables energy conservation and facilitates bidirectional current flow. SPWM governs the sequence of switch activation and deactivation by juxtaposing a sinusoidal reference signal with a high-frequency triangular carrier.

This comparison establishes the duty cycle and switching timings, resulting in modulated pulses that resemble a sine wave output. The architecture is symmetrical, facilitating management and ensuring consistent voltage across phases. This indicates its applicability for both grid-connected and off-grid AC applications.

2.1 Design Equations

There are a few basic equations that are used to look at and rate the inverter's performance. Ohm's Law in Eq. (1) is used to figure out the current load. It does this by looking at the output voltage and resistance and figuring out how much current is flowing through the load. The output power comes from Eq. (2), which determines how much power the inverter can deliver. The fundamental output voltage produced by sinusoidal PWM (SPWM) is estimated to be used in Eq. (3), where the modulation index and DC input voltage are considered. For filter design, the LC low-pass filter is tuned using the formula in Eq. (4), which ensures that the fundamental frequency passes while higher-order harmonics are attenuated; this also allows the inductor value to be determined when capacitance and cutoff frequency are known. Finally, waveform quality is evaluated using Total Harmonic Distortion (THD), calculated in Eq. (5), which quantifies how much harmonic distortion is present relative to the fundamental output voltage.

$$I = \frac{Vs}{R} \tag{1}$$

$$P_o = \frac{V^2}{R} \tag{2}$$

$$V_o = m_a \times VDC \tag{3}$$

$$f_c = \frac{1}{2\pi\sqrt{LC}} = L = \frac{1}{(2\pi f_c)^2 C} \tag{4}$$

$$THD = \frac{\sqrt{Sum\ of\ Harmonics^2}}{Fundumental\ V_o} \tag{5}$$

2.2 Filter Design Analysis

To improve the inverter output waveform and lower harmonic distortion, a passive LC low-pass filter was built. The filter lets the 50 Hz fundamental frequency through but blocks higher-order harmonics from getting through. The inverter makes these harmonics when it turns on and off. The cutoff frequency is set just above the fundamental frequency to make sure that there is as little distortion as possible. Using equation (4), the inductance value is found with a capacitance of 4.7 µF and a cutoff frequency of 1000 Hz. The inductance is about 5.4 mH. As shown by the simulation, this LC filter setup does a good job of smoothing out the inverter output and keeping the THD level below 5%. The parameters chosen are the best balance between how well the filter works and how easy it is to use [4].

2.3 Component Selection

This inverter design includes a number of parts that are critical to its performance. The main switching devices are MOSFETs, which were preferred to IGBTs because of faster switching times, lower losses during conduction, and compatibility with medium voltage systems. Each of the MOSFETs used in this design can sustain greater than

6 A currents and is rated at over 1000 V, which perfectly matches the need in this design for 1000 VDC input and load. Their rapid turning on and off capability makes them ideal for high-frequency SPWM operation. To filter the output signal, a film capacitor of 4.7μF is used. Due to low ESR, film capacitors can improve the shape of the signal, reduce high-frequency noise, and smooth the output wave. The inductor in the LC output filter has been estimated to be around 5.4 mH, which will yield a cutoff frequency of about 1000 Hz, letting through the 50 Hz fundamental frequency while greatly suppressing higher-order harmonic frequencies. In addition, the inductor is estimated to be able to provide at least 6 A of current without magnetic saturation. At the output of the inverter, the output is emulated by a balanced RL load with a resistor value of 10 ohms. This resistor value is selected based on the anticipated output voltage and current, as well as a proper power rating to guarantee safety and stability during simulation tests [5].

3. Methodology

Fig.1 shows the flowchart of the simulation and analysis of the three-phase multilevel inverter system, which was carried out using PLECS, focusing on the implementation of Sinusoidal Pulse Width Modulation (SPWM) and passive filter design. The system was configured to operate with a DC input voltage of 1000 V, and the desired output frequency was set to 50 Hz, aligned with standard Malaysian electrical systems. A 6 kHz triangular waveform was used as the carrier signal for the SPWM technique, and the modulation index was chosen as 0.9 to optimize output voltage while preventing overmodulation. The load on each phase was modeled as a 10 Ω resistive element, forming a balanced three-phase RL load when combined with the LC filter components.

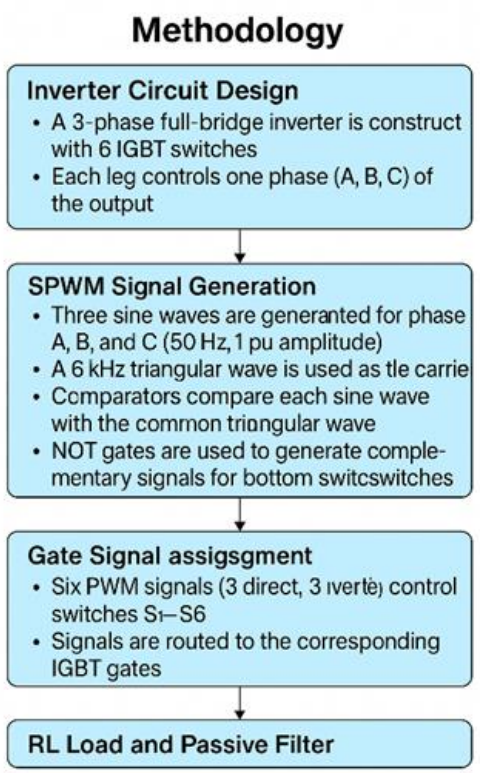

Fig. 1 *The project methodology flowchart*

3.1 SPWM Switching Strategy

In general, the three arms of this inverter will be delayed by 120 degrees to produce a 3-phase AC supply. The switches used in the inverter have a 50% ratio, and switching can occur after every 60-degree angle. Switches such as S1, S2, S3, S4, S5, and S6 will complement one another. In this case, three single-phase inverters are connected to a similar DC source. The pole voltages in a 3-phase inverter are equivalent to the pole voltages in a single-phase half-bridge inverter [5][6]. The conventional 3-phase inverter has six switches labelled S1, S2, S3, S4, S5, and S6, as shown in Fig. 2.

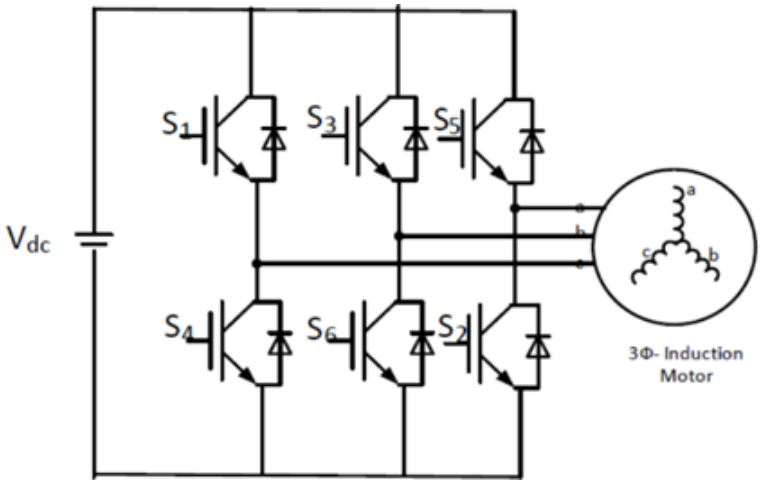

Fig. 2 *The 3-phase switch inverter technology*

The SPWM strategy was implemented by generating three reference sine waves (each phase shifted by 120°) and comparing them with a common high-frequency triangular carrier signal. This comparison generated six gate signals, three for the upper MOSFET switches and three inverted signals for the lower switches, ensuring proper complementary switching without overlapping. These gate signals controlled the switching of the MOSFETs in each leg of the inverter.

3.2 Filter Design Parameters

Based on a cutoff frequency of 1000 Hz, a 4.7 μF capacitor and a 5.4 mH inductor were used to make a low-pass LC filter, as shown in Table 1. To get rid of high-frequency harmonics caused by the switching operation, the filter was linked to the output of each inverter leg.

Table 1 *LC filter parameters*

Parameter	Value
Capacitance (C)	4.7e-6 F
Cut Off Frequency	1000 Hz
Inductance (L)	5.4e-3 H

3.3 Simulation Procedure

The first step in the simulation is to make the PLECS design for the three-phase multilevel inverter. Each leg has two MOSFET switches, one for each phase (A, B, and C). There were also anti-parallel diodes on each leg that let the current flow in both directions. The DC link was set to 1000 VDC, and each leg was connected to its own output node [7].

Secondly, as shown in Fig. 3, the SPWM control system was created. Three sinusoidal reference signals were created, one for each phase. Each one is moving 120° from the one before it. At 50 Hz, these signals demonstrate what the right basic output was. Then the PWM gate signals for the upper switches (S1, S3, and S5) were compared to a triangle carrier waveform that had a frequency of 6 kHz. The logical NOT gates send signals that are the opposite of what the lower switches (S2, S4, and S6) were sending. This blocks the switches from getting in each other's way and halts shoot-through from happening.

After designing the inverter and control, a passive LC filter was added to each output phase. There is a 5.4 mH inductor and a 4.7 μF capacitor in the filter. Choosing these filter parts because their design will let the 50 Hz fundamental frequency through while cutting down on switching harmonics, as shown in Fig. 4.

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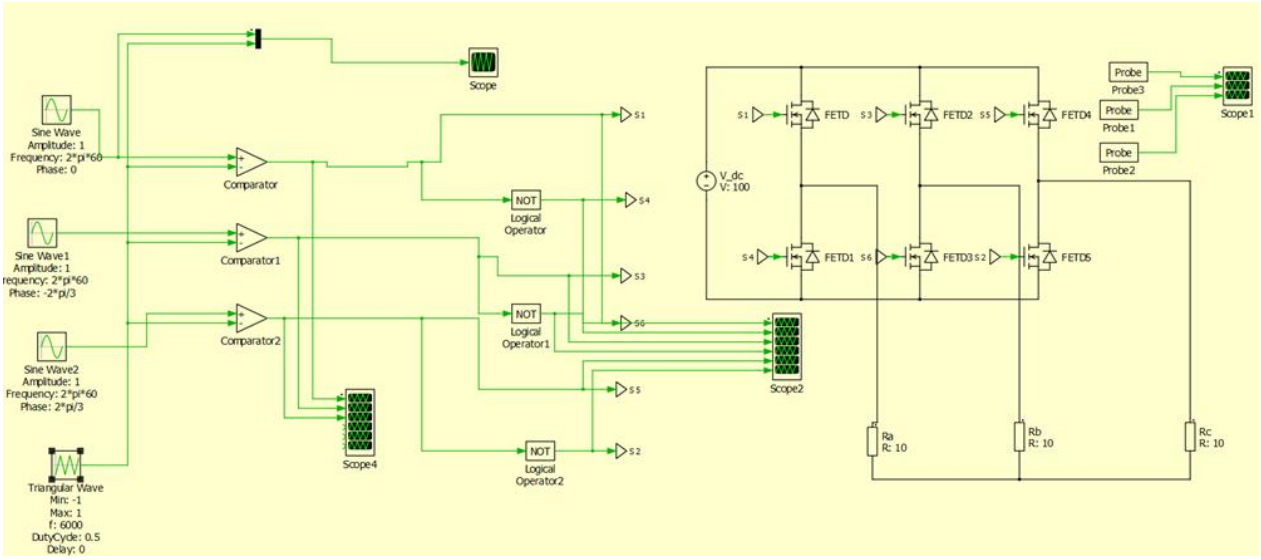

Fig. 3 *The 3-phase inverter with six switches*

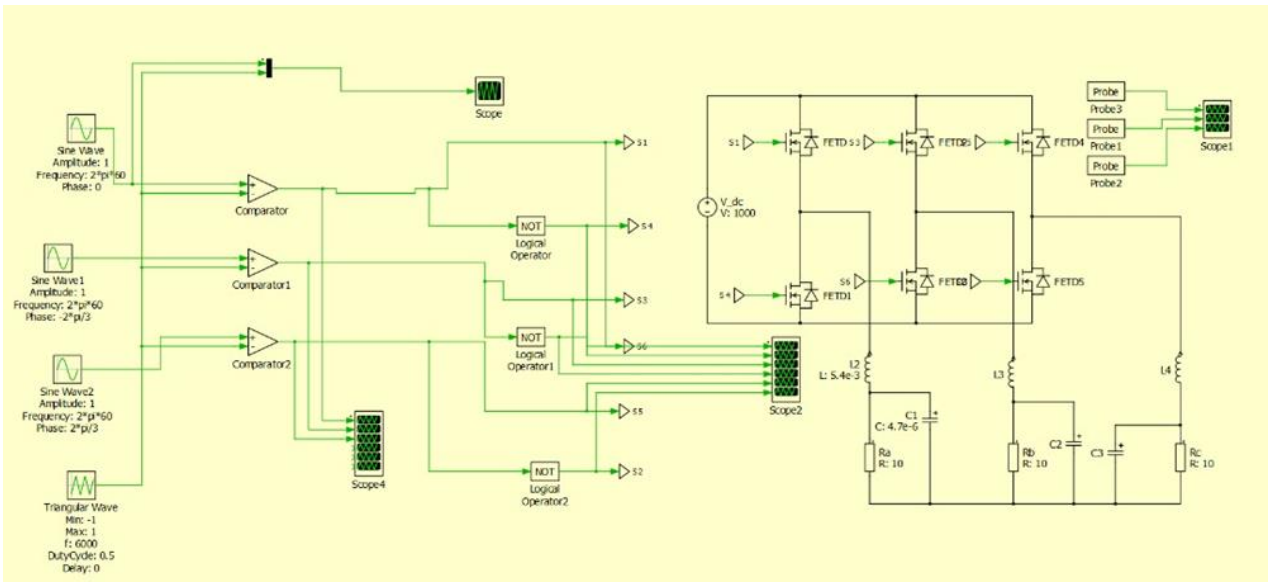

Fig. 4 *The 3-phase inverter with LC filter*

4. Results and Discussion

As shown in Fig. 5 and 6, the model of a three-phase system was simulated in PLECS software. It generates three sine waves, each 120° apart. A 1000V DC input is supplied with six switches arranged in three inverters connected with an R load using SPWM. The circuit uses three sine waves, and a triangular wave is used as a carrier signal. By using these parameters, ensure accurate SPWM generation, produce a balanced three-phase AC output. Fig. 6 shows the output waveforms of a three-phase AC inverter.

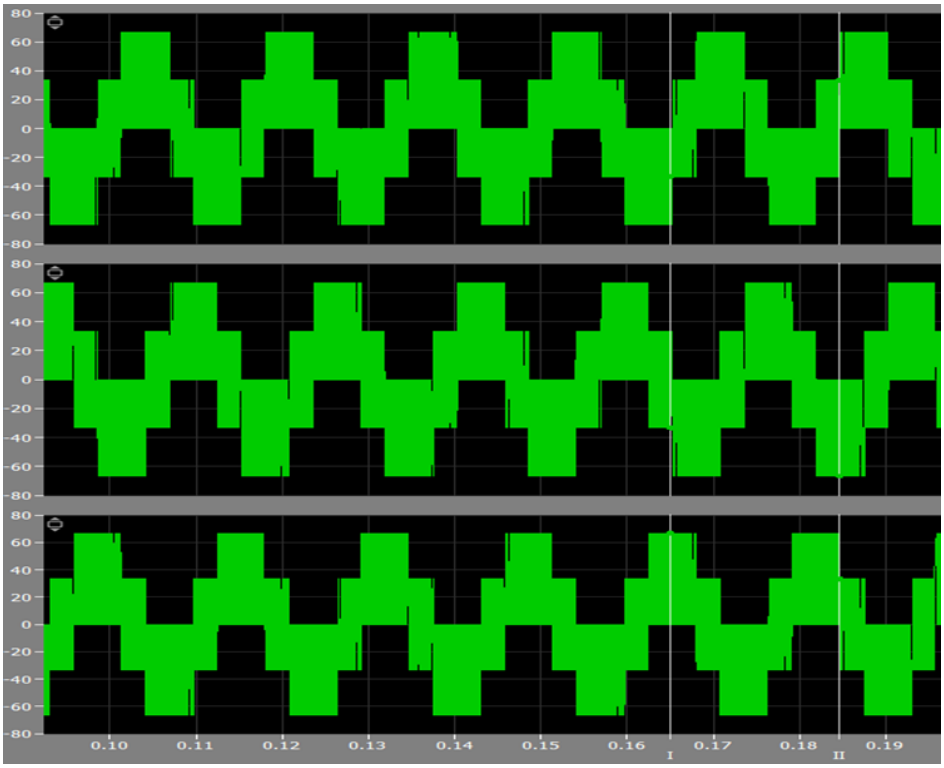

Fig. 5 *Output of the AC inverter*

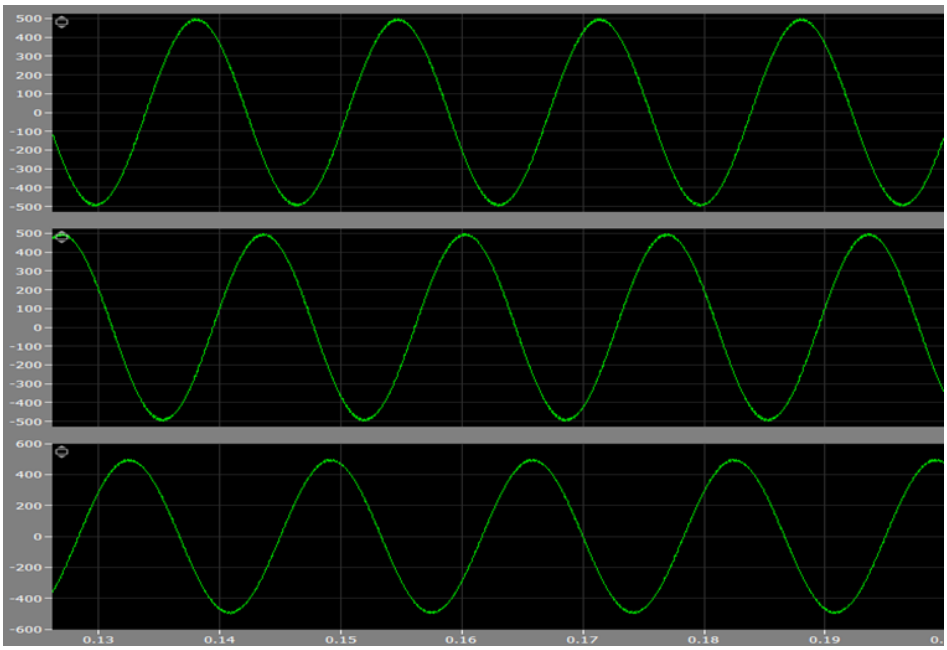

Fig. 6 *Output of AC with LC filter*

Fig. 6 shows the output waveforms of a three-phase AC inverter after adding a filter. Meanwhile, Table 2 shows how LC filtering affects the quality of the inverter's output voltage. After using the filter, the RMS voltage drops noticeably in all three phases. The main reason for this drop is that high-frequency harmonic components, which used to add to the total RMS value, have been removed. By reducing these harmonics, the LC filter smooths out the waveform, which makes the output more sinusoidal. Also, small voltage drops across the inductor may play a role in this change. Even though the RMS voltage goes down a little, the Total Harmonic Distortion (THD) goes down a lot, to less than 1.2%. This shows that the filter works to improve the quality of the output waveform and meets the goal of less than 5% THD.

Table 2 *THD comparison*

Phase	RMS Voltage (V)	THD before filtering (%)	THD after filtering (%)
Ra	427.104	68.96%	1.12%
Rb	431.392	68.01%	1.02%
Rc	427.816	68.47%	1.02%

5. Conclusion

This project shows how to build, simulate, and test the performance of a three-phase symmetric multilevel inverter that uses Sinusoidal Pulse Width Modulation (SPWM) with an R-load. PLECS was used to model the inverter and added an LC filter to cut down on output harmonics. The simulation results demonstrate that the system works well and that the waveform quality is much better after filtering, with the THD going from more than 68% to less than 1.5%. The resulting design satisfies all the requirements, which shows that the selected topology with LC filter configuration effectively suppresses the harmonics, indicating the suitability for grid-connected and industrial power conversion.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The author confirms sole responsibility for the following: study conception and design, data collection, analysis and interpretation of results, and manuscript preparation.

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