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Electronic Abacus (e-Abacus) using FPGA Altera DE2 Board

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Abstract: The development of electronic abacus using Altera DE2 115, is to integrate the use of abacus along with electronic devices which offer better visualisation of the abacus operations. The main focus of this technology is to assist the primary school students in validating a fundamental arithmetic operation. The electronic abacus is developed by integrating an abacus, abacus decoder module and field programming gate array (FPGA) based processor. DE2 115 is chosen as the development module and very high-speed integrated circuit hardware description language (VHDL) as a main programming language. The arithmetic algorithm developed for the electronic abacus is limited to the computational of whole numbers only, involving the basic arithmetic operation of additional, subtraction, multiplication and division. This electronic abacus comes with two operational modes, display and arithmetic mode. In the display mode, the abacus beads position at column one until column seven is displayed as numerical representation on the liquid crystal display (LCD) screen. A computation of arithmetic operations with less than three operators is available in the arithmetic mode with the capability of displaying the negative numerical and infinite value. From the simulation conducted in Quartus II, the implementation of the algorithm in FPGA utilise 4% from the total logical element allowed and consume approximately 143.4 mW of power. As a conclusion, this enhanced ancient apparatus hopefully will contribute to the development of more lively and interesting teaching approach.

Keywords: Electronic abacus; FPGA; Altera DE2; VHDL; Arithmetic operation

1. Introduction

The practice of traditional abacus as a brain stimuli has been known worldwide and proven to be an effective method in the mathematical learning process. Learning a traditional abacus without the presence of a teacher is proven to be a hassle, as it requires a different technique for different mathematical operation. This drawback has been acknowledged by the researcher, and the development of computerized module related to abacus usage for the young and old has filled the gap.

The invention of Indian Abacus [1] is a hardware based electronic abacus. The function of abacus is emulated by a 13×5 grid of sliding switches. The computational result is later displayed on LCD screen or sent via USB, in order for the result to be posted on the internet. This capability enables the Indian Abacus to be used in primary and secondary abacus competition, thus emphasized as educational tools. Electronic abacus proposed by Alison Barker [2], is equipped with electronic sensors which detect the abacus bead position and transmit the data through USB and displayed on the computer screen. The additional features of audible capabilities and magnified text enable this prototype to be used by visually impaired personnel and normal person as well. The development of E-Abacus [3], demonstrate the integration of traditional abacus with the use of sensors and microcontroller. This integration produces flexible application and enabling the abacus to be operated individually or with the aid of microcontroller computation.

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The ability to display the numerical representation according to abacus bead positions and result from an arithmetic operation on LCD screen is the distinctive features of this invention.

The development of electronic abacus presented in this paper is an approach to validating a mathematical operation conducted by an abacus, without missing the physical experience of using the actual apparatus. It is designed as additional apparatus which can be detached while not in use, is preserving the abacus authenticity [4, 5]. The development of electronic abacus algorithm using VHDL programming language is chosen due to better digital design flexibility and synthesizable register transfer level (RTL) which later can be used to develop its specific function of the integrated circuit [6]. The development of this electronics abacus could promote a better understanding and active learning process in mathematical courses for kindergarten, schools student as well as adult learners [7].

2. Electronic Abacus

The system of electronic abacus consists of (1) an abacus, (2) abacus bead sensor board which decode the bead position into numeral values, both will acts as the external hardware that provides input to the DE2 interface board, (3) DE2 interface board that interface abacus bead sensor board to the main processor, by sending the data through GPIO port, and (4) DE2 board which compute the algorithm thus provide the external input and VHDL programming software, it also serves as the central processing unit which computes the numerical representation from abacus bead position. Fig. 1 illustrates the layout of electronic abacus system.

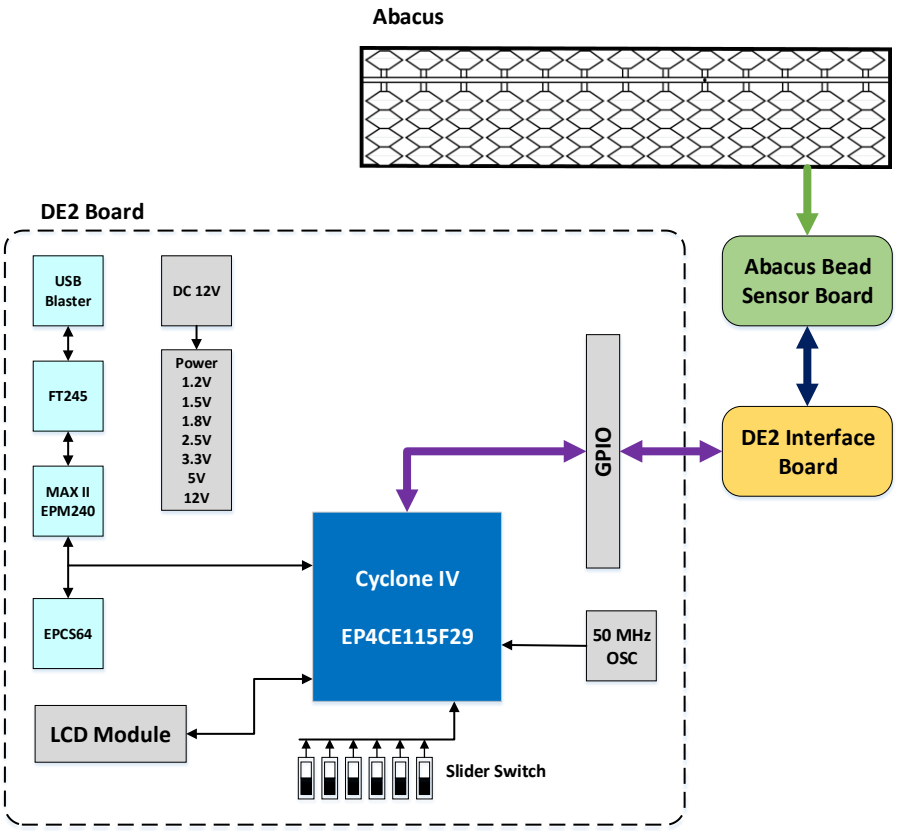


Fig. 1 - Electronic abacus layout

2.1 Enhanced Job Ranking Backfilling Model

The bead sensor board is dimensioned respective to the abacus hollow inner dimension, served as the locking mechanism to ensure the abacus is static during operation. Reflective interrupter SH9206 is used as the abacus proximity bead sensor. This will enable the design to detect the presence of abacus bead without any physical contact while keeping minimal distance between the sensors with abacus bead. The packaging of this device allows a precision fitting in a concise space and due to the use of surface mount component, the position of the sensors will be uniform. The sensors are aligned into 13×5 matrix grid and positioned precisely according to the center of bead position in rows and columns. The positioning of the bead to the respective sensor is demonstrated in Fig. 2 (a).

As bead sensor is positioned with the closest proximity as possible to the abacus bead, an optimal value of the resistor that limits the current flowing through each sensor should be obtained. The selection of resistor value for current limiter is crucial in ensuring that the overall sensor circuit will produce a viable logic level during its operation.

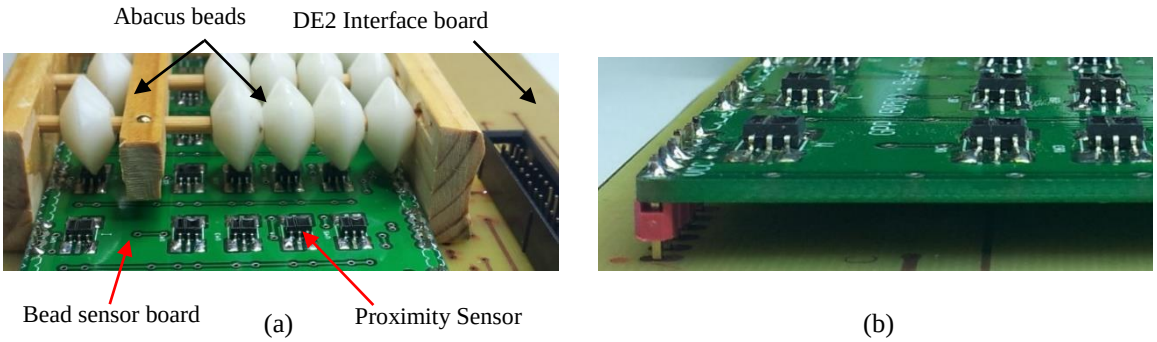


Fig. 2 (a) Multistage board configuration with respect to abacus bead, (b) Bead sensor board elevation

2.2 DE2 Interface

The prime function of DE2 interface board is to provide interconnection between bead sensor board and FPGA-based processor. The secondary function is to provide an elevation to the bead sensor board thus ensuring the minimum distance between abacus beads and abacus bead sensor. The elevation distance provided by the DE2 board interface is illustrated in Fig. 2 (b) will ensure the proper digital reference produced by the sensor in detecting the abacus bead.

2.3 Arithmetic Algorithm

The algorithm of the overall function is sectioned into two; which are display and arithmetic mode. The display mode portrays the mathematical numerical representation in accordance with abacus bead position. The arithmetic mode can be selected to operate with two variables or three variables. The two variables mode operation will conduct addition, subtraction, multiplication and division operations of two variables at one time. Meanwhile, the three variables mode can be operated with the combination of two arithmetic operations. Total of 16 arithmetic combinations is possible when the abacus is operated in three variables mode. The flowchart of the overall process is illustrated as in Fig. 3 (a) and (b).

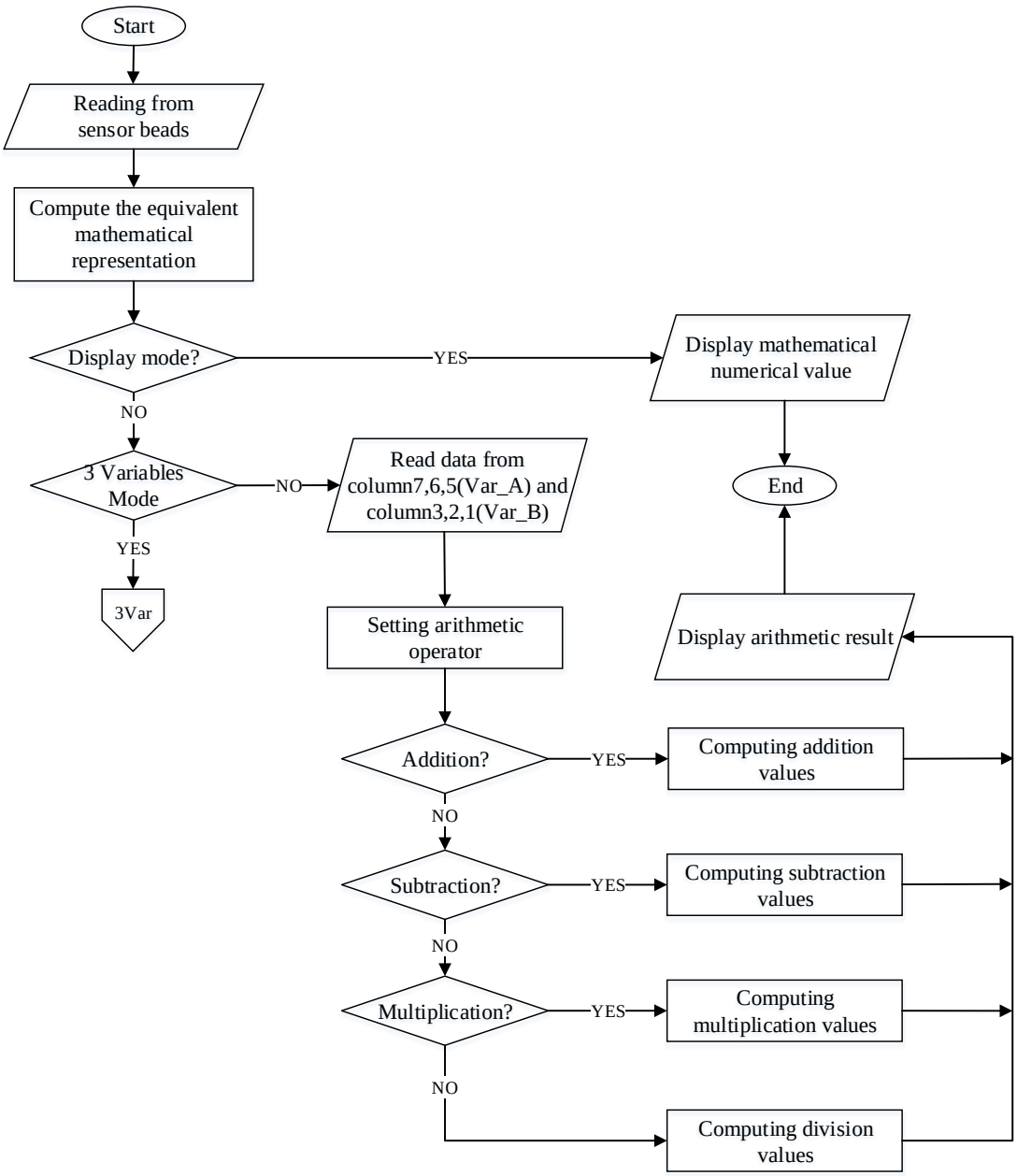


Fig. 3 (a) - Flowchart of two variables arithmetic and display modes

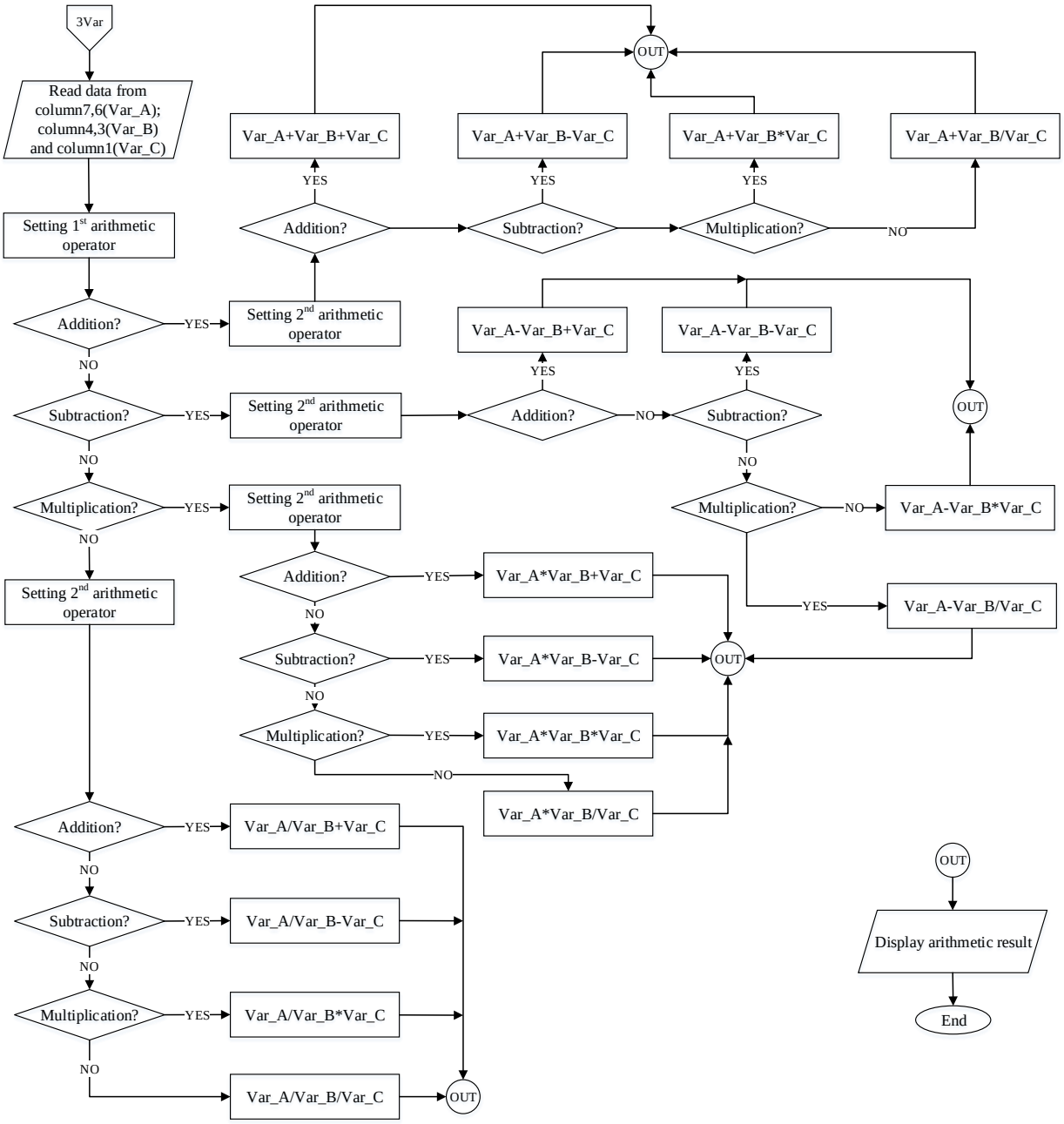


Fig. 3 (b) - Flowchart of three variables arithmetic mode

Moreover, to understand the overall proposed model, the flowchart in Fig. 2 is used. Each job submitted to the scheduler contains three variables including number of CPUs, memory size and average CPU speed. The first step of building the enhanced job ranking backfilling model is to propose two ranking equations to rank the jobs based on linear function and logarithmic function. The ranking equations, after that, is used to rank the incoming jobs and store the rank value with the job's variables in the queue. The scheduler chooses the smallest ranked job in the queue to be served by resource.

3. Simulation of Arithmetic Algorithm

The arithmetic algorithm developed using VHDL was tested using ModelSim. The arithmetic algorithm is available for two variables and three variables arithmetic computation. Two variables mode will compute a designated arithmetic operation for a three digits numeral for each variable. Whereas in the three variables mode, a combinational operation for two variables with two digit numerals and a single digit numeral will be carried out.

For two variables arithmetic operations, the first variable is taken from abacus column 7, 6 and 5, while abacus column 3, 2 and 1 are set as the second variable. The simulation output for two variables is illustrated as in Fig. 4 (a).

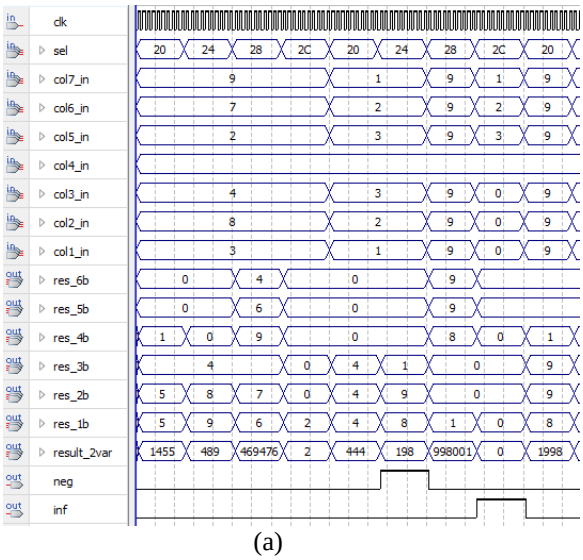
The sel (selector) flag is to indicate the simulation output, which are each sel value represent one unique operator. Value of 20, 24, 28 and 2C, indicated the computation of the additional, subtraction, multiplication, and division operation, respectively. For example, the operation of 321 - 123 which is indicated at sel flag 24, resulted in a computational value of 198 with neg enable. Neg is a flag to indicate the negative numerical value and used to mark the signage display on the LCD screen. Another flag of inf is used to notify the system during a divide by zero operation. The infinite flag of inf will be enabled when the divisor value is equal to zero.

Meanwhile, for three variables arithmetic operations, each variable are separated by a void column. The first void column is located at column 5 which separated the first and second variable. The first variable is taken from abacus column 7 and 6, while abacus column 4 and 3 makes the second variable. Each of these variables will have a maximum value of 99. The second void column is located at column 2, separated the second variable and the third variable. The third variable is only a single digit which has the maximum value of 9. The simulation for three variables arithmetic is illustrated in Fig. 4 (b), (c), (d) and (e).

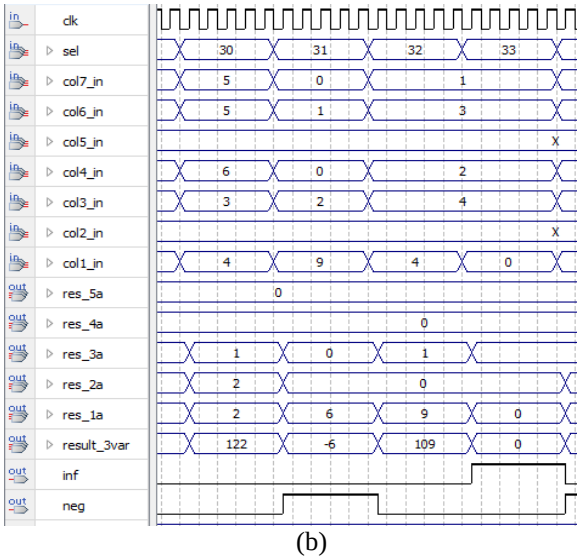
Fig. 4 (b) demonstrate the simulation output with the implementation of setting additional as the first operator and another operator as the second operator. Referring to Fig. 4 (b), the first sequence demonstrated the operation of a double addition of 55+63+4 which have the computational result of 122. The second sequence demonstrates the subtraction as the second operator. While third sequence shows that the second operator is a multiplication and the fourth sequence is division operator.

Fig. 4 (c) demonstrate the simulation output with the implementation of setting subtraction as the first operator and another operator as the second operator. The sequence of the second operator is similar to the sequence discussed earlier. An example of multiple subtractions is demonstrated by 20-35-3 which produced a computational value of 18 with negative flag enable. Fig. 4 (d) demonstrate the simulation output with the implementation of setting multiplication as the first operator and another operator as the second operator. The simulation result of the third sequence with the value of 3402 is from the arithmetic operation of 18*21*9. Fig. 4 (e) demonstrate the simulation output with the implementation of the setting division as the first operator and another operator as the second operator. The simulation result of the third sequence with the value of 0 and infinite flag enable is from the arithmetic operation of 32/00*8.

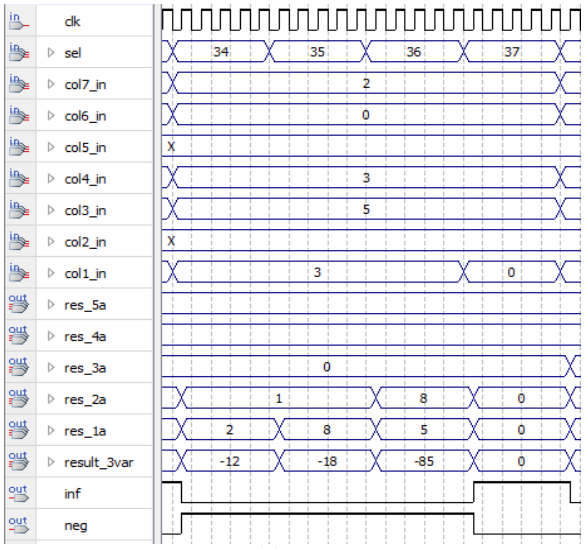
The algorithm is designed for computation of whole numbers only. The fractional result will not be displayed. The abacus input is only considering the whole number columns. Thus, will discard the five columns from the right. Due to the limitation of the input port to DE2 board the left most column is also discarded. This implementation only considering the abacus column from the unit column (referred as column 1) to million column (referred as column 7).



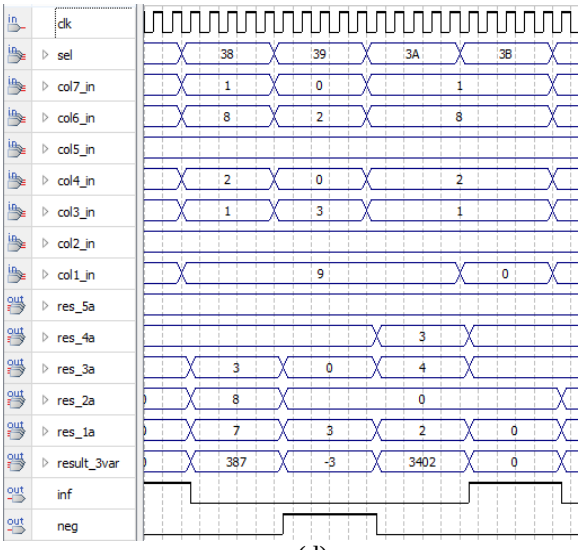
(a)



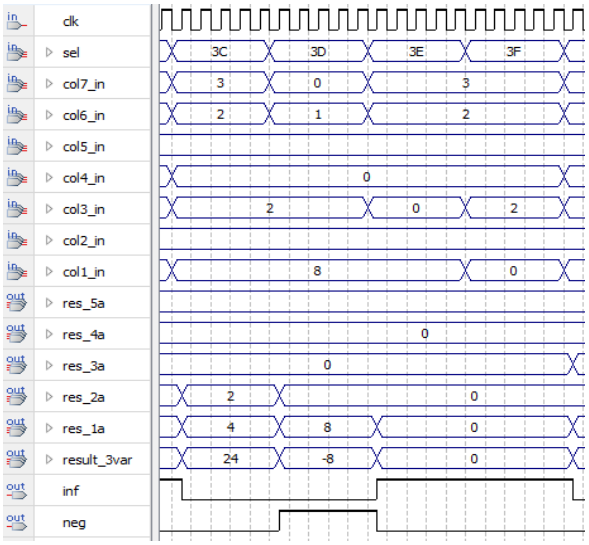
(b)



(c)



(d)



(e)

Fig. 4 - Simulation output of, (a) two variables arithmetic, (b) addition combinations, (c) subtraction combinations, (d) multiplication combinations and (e) division combinations.

4. Simulation of Arithmetic Algorithm

In display mode, the electronic abacus will able to display a seven digits numeral representation in accordance with the bead placement in column 1 until column 7. The algorithm is designed to decode the bead placement according to its respective column and placed the numeral value in decimal position on the LCD screen.

Each mode performed by electronic abacus is indicated by a different notation at the first line on the LCD screen. The display mode is indicated by the display of "Numerical Value:". Two variables arithmetic mode is noted by the operational function of its arithmetic operator whether it is additional ("Add."), subtraction ("Subt."), multiplication ("Mult.") or division ("Div."). The three variables arithmetic is indicated by the displaying of "Func." on the first line of the LCD screen. Fig. 5 illustrates the implementation of such notation according to its designated mode.

The arithmetic algorithm is designed to perform in whole number computations. Each parameter is read separately from its respective columns and combined as a designated variables. These variables are then computed in accordance with the selections of an arithmetic operator. The numerical result is stored in a temporary memory and split into a separate numeral representations in accordance to its decimal digits. These digits are later converted to ASCII representation and store in a string of arrays which later used as the display character on the LCD screen.

The implementation of abacus algorithm on the electronic abacus complement its simulation result. The development of the algorithm using VHDL offers precise bit manipulation and variation of algorithm architecture in comparison with conventional microprocessor programming language.

5. Conclusion

The electronic abacus presented in this paper is capable to process the representation of the whole number for 7 digits and arithmetic operations with less than three operators. The implementation of electronic abacus using DE2 board proven to be a better alternative in the advancement of the algorithm. Precise simulation output offers by Modelsim simulator enable the algorithm to be rectified and optimized at design entry level thus reducing the implementation hiccup at the hardware level. The arithmetic computation carried out by the algorithm, involves only whole numbers. The implementation of the arithmetic operator such as addition, subtraction and multiplication will be similar compared to conventional method. The arithmetic computation involves division operator will produce a whole number value without displaying its remainder or resulting in a fractional value. However, the arithmetic operation involving division operator need to be explained accordingly to prevent confusion to the users. The detachable features of abacus with the concise design is the key features of this design. A reminder to place the abacus beads with proper alignment for each abacus column to prevent an error in numeral display and numerical computation.

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