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Characteristics of High Voltage Gain of Non-Isolated Inductor-Less DC-DC Converter

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Abstract: The main purpose of this study is to analyze a multilevel DC-DC converter structure for achieving high voltage gain of DC-DC converter. The Inductor-less Multistage Modular Capacitor Clamped DC-DC Converter (IMMCCC) is one of the multilevel structure that can achieve the high voltage gain. In this circuit structure, the concept of charging and discharging capacitors is used in order to achieve high voltage gain regardless of the duty cycle influence. For the conventional DC-DC boost converter, the output voltage depends on the duty cycle, where high voltage gain is not practically achievable even though with a high duty cycle. Thus, the multistage structure which is IMMCCC is selected in order to achieve the high voltage gain of DC-DC converter. In order to analyze and confirm principle of the designed converter, simulation and experimental works are conducted. Three structures i.e., one, two and three stages of the IMMCCC are designed and constructed. Based on the experimental results, the obtained output voltages are 60 V (boost ratio = 2), 90 V (boost ratio = 3) and 120 V (boost ratio = 4) with the input voltage of 30 V. From the simulation and experimental results, the operation of the designed IMMCCC is confirmed.

Keywords: DC-DC converter, multilevel, multistage, high voltage gain, capacitor clamped, inductor-less

1. Introduction

In recent years, DC-DC converters are widely used in many applications such as electrical vehicle (EV), DC-DC transmission line, telecommunication data center [1][2]. The input voltage of the generation such as photovoltaic is typically low and unregulated. Hence, a suitable converter is required in order to increase the output voltage. The conventional DC-DC boost converter is practically not able to generate very high output voltage because it requires high turn-on duty cycle [3]. Very high duty cycle causes the turn-off switching time becomes narrow and it would cause the switching devices to be always in ON condition. Furthermore, it causes the increasing of conduction loss and the rating (current/voltage) for the components [4]. Besides, very high duty cycle, beyond 0.8 also increases switching loss [2], [4], [5]. Very high voltage gain is required for converting very low source voltage to very high output voltage, such as from 10 V to 100 V. In order to overcome this problem, multistage or multilevel structures of DC-DC converter are required in order to achieve the high voltage gain without concerning the duty cycle issue [6]–[10]. Thus, the selection of inductor-less multistage modular capacitor clamped DC-DC converter (IMMCCC) circuit structure is considered in this study, whereby with this structure high voltage gain can be achieved without concerning duty cycle issue.

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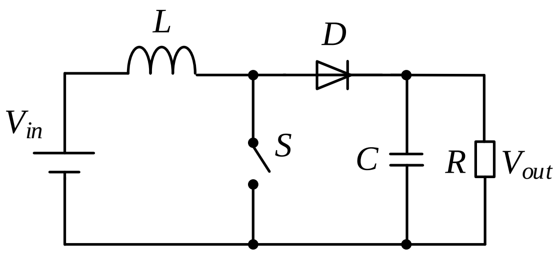
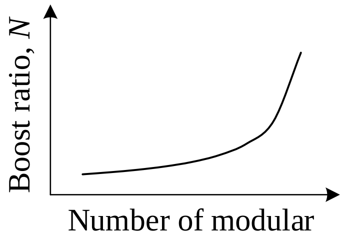
2. Conventional DC-DC Boost Converter

Conventional DC-DC boost converter is one of the simplest circuit that able to boost-up from low to higher voltages. Fig. 1 shows the conventional DC-DC boost converter circuit and the output voltage depends on the duty cycle [1]. Meanwhile, Fig. 2(b) shows the relationship of boost ratio and duty cycle. The DC-DC boost converters can be operated in two conditions, i.e., continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [11]..



(a) Circuit structure



(b) boost ratio vs duty cycle

Fig. 1 - Conventional DC-DC converter

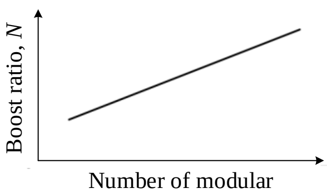
3. IMMCCC Designs Consideration

For this structure, the energy is transferred from input to the output sides through several capacitor components [12]. The concept of charging and discharging of capacitors is applied in order to achieve the high voltage gain of DC-DC converter. For the IMMCCC, number of stages are referred to (N – 1), where N is the boost ratio [13]. Meanwhile, the number of stages must be increased if higher output voltage is required with duty cycle of 0.5. The output voltage can be obtained by referring Equation (1). Fig. 2 shows IMMCCC boost ratio versus number of modular, and modular block arrangement in cascaded configuration.

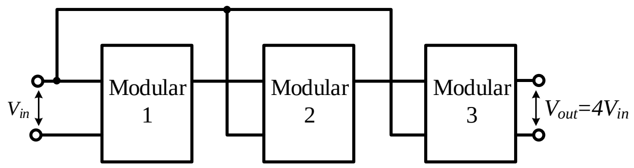
Fig. 3(a) shows the single IMMCCC block that consists of one capacitor and three switching devices. For an example, one modular block generates output voltage of two times of the input voltage. For the switching scheme of IMMCCC, it requires only two operation modes with delay angle of 180° one another and the duty cycle is fixed at 0.5, Fig. 3(b).

Fig. 4 shows the operation mode of the three-stage of IMMCCC. During Mode I, all switches S_p are ON, capacitors C_1 and C_3 are charging, and C_2 is discharging. Meanwhile, during Mode II, all switches Sn are ON, capacitors C_1 and C_3 are discharging, and C_2 is charging. The output voltage is step-up through the process of charging and discharging of the capacitors.

$$V_{out} = V_{in}(N-1) \tag{1}$$

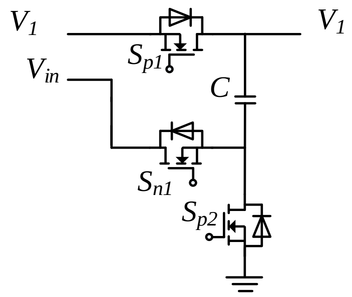


(a) Boost ratio vs number of modular

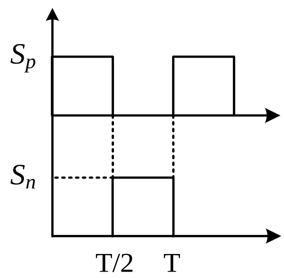


(b) Modular block arrangement

Fig. 2 - IMMCCC concept

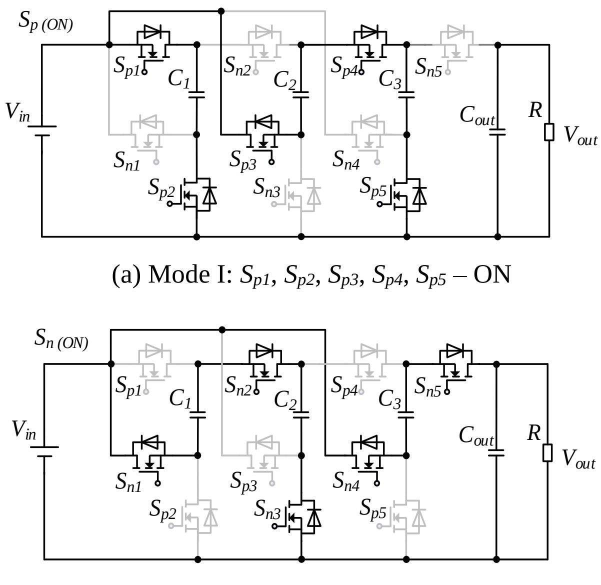


(a) Single block [12],[13],[14],[15]



(b) Switching scheme

Fig. 3 - IMMCCC implementation



(a) Mode I: S_{p1}, S_{p2}, S_{p3}, S_{p4}, S_{p5} – ON

(b) Mode II: S_{n1}, S_{n2}, S_{n3}, S_{n4}, S_{n5} – ON

Fig. 4 - Operation mode of three-stage IMMCCC

3.1 Resonant IMMCCC for Soft-Switching Achievement

Generally, circuit structure of resonant IMMCCC is similar to the non-resonant IMMCCC structure. However, it requires a stray inductor at each stage in series as a resonant tank. Soft-switching can be realized by considering resonant IMMCCCs, thus switching loss of semiconductor devices is reduced [14]–[15]. Fig. 5(a) shows the three-stage of resonant IMMCCC. Each stray inductor is based on the switching frequency and the stage capacitors, C_1 or C_2 or C_3. In this case, switching frequency is same to the resonant frequency by referring the current loop during Mode I and Mode II, Equation. (2). The stage capacitor at each stage is estimated based on equation (3). Meanwhile, for the stray inductor, $2L_{S1} = L_{S2} = L_{S3} = L_{S4}$, whereby L_{S1} is expressed by Equation (4).

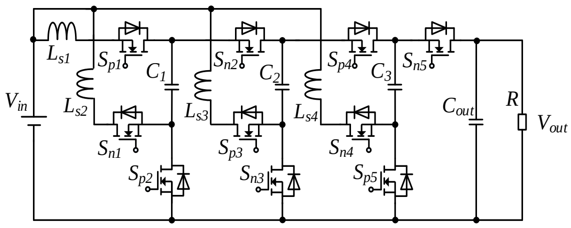
$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

$$C = \frac{\pi P_{out}}{4V_{in}\Delta v_c \omega_r} \tag{3}$$

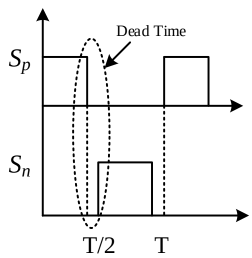
$$L_{S1} = \frac{1}{C(2\pi f_s)^2} \tag{4}$$

Switching scheme for resonant IMMCCC is similar as non-resonant IMMCCC, however it requires appropriate dead-time during Mode I and Mode II transition. The dead time is estimated based on Equation (5). Fig. 5(b) shows the switching scheme with dead time.

$$T_d = percent\left(\frac{1}{f_s}\right) \tag{5}$$



(a) Three-stage



(b) switching scheme with dead time

Fig. 5 - Resonant IMMCCC

4. Results and Analysis

The simulation results are analyzed for the conventional DC-DC boost converter, IMMCCC and resonant IMMCCC. Meanwhile, for experimental results, only conventional DC-DC boost converter and IMMCCC are concerned.

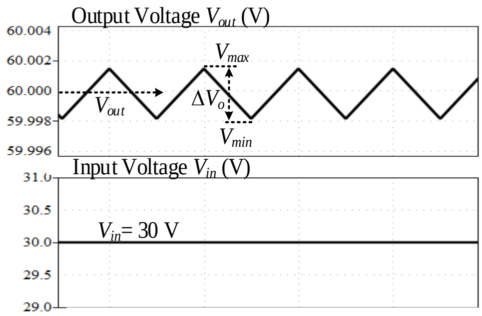
4.1 Conventional DC-DC Boost Converter Result

Table 1 shows the prescribed specifications of the conventional DC-DC converter. Only CCM is considered in this study.

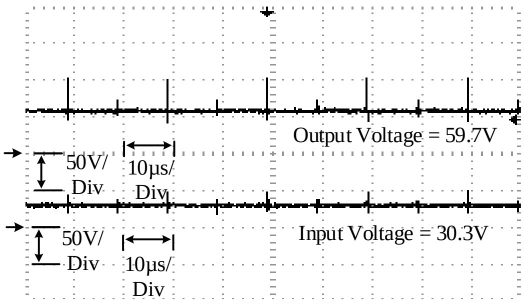
Table 1 - Experimental and simulation specifications of conventional DC-DC boost converter

Parameters	Value
Input voltage, V_{in} (V)	30
Output voltage, V_{out} (V)	60
Load, R (Ω)	150
Inductor, L (mH)	1
Capacitor, C (μF)	1200
Switching frequency, f_s (kHz)	50
Duty cycle, D	0.5

Fig. 6 shows the simulation and experimental results of the conventional DC-DC converter. The output voltage is approximately 60 V for the input voltage is 30 V. Both results show a good agreement, between simulation and experimental results. Thus, the design principle of the conventional DC-DC converter parameters are confirmed.



(a) Simulation



(b) Experiment

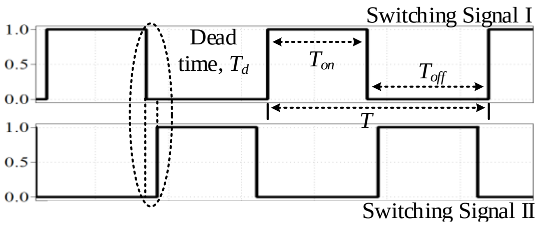
Fig. 6 - Simulation and experimental results of the input and output voltages

4.2 IMMCCC Results

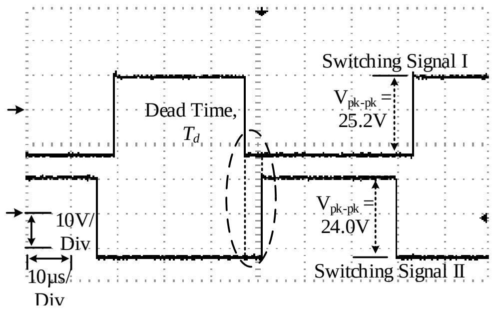
Table 2 shows the specifications of the one-stage, two-stage and three-stage of IMMCCCs for simulation and experimental setups. Fig. 7 shows the switching signal with dead time arrangement for simulation and experiment setups. The dead time is estimated 5% of the switching period. For the experimental setup, the switching period, T is approximately 32 μs and the dead time, T_d time is 1.8 μs, Fig. 7(b). Fig. 8 shows the experimental results of the one-stage, two-stage and three-stage of the IMMCCCs. The input voltage is 30 V for one-stage and two-stage IMMCCCs for the output voltages of approximately, 60 V and 90 V, respectively. Meanwhile for the three-stage IMMCCC, the output voltage is 10 V for the output voltage is approximately 40 V. All the results show good agreement with the principle of the one-stage, two-stage and three-stage IMMCCCs, i.e., one-stage ($V_o = 2V_{in}$), two-stage ($V_o = 3V_{in}$) and three-stage ($V_o = 4V_{in}$). The input and output voltage ratings for the three-stage IMMCCC are reduced due to the components voltage rating limitation.

Table 1 - Experimental and simulation specifications of conventional DC-DC boost

Parameters	Value
Input voltage, V_{in} (V)	30
Duty cycle, D	0.5
Switching frequency, f_{sw} (kHz)	31
Capacitor, C (μF)	1000
Dead Time, T_d (%)	5

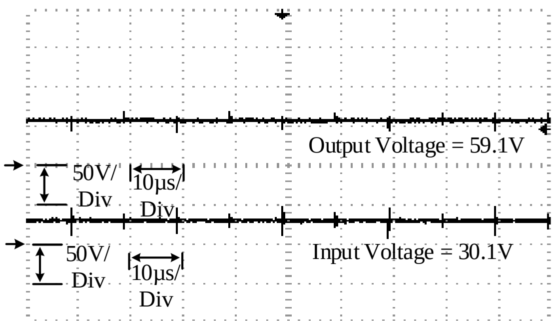


(a) Simulation

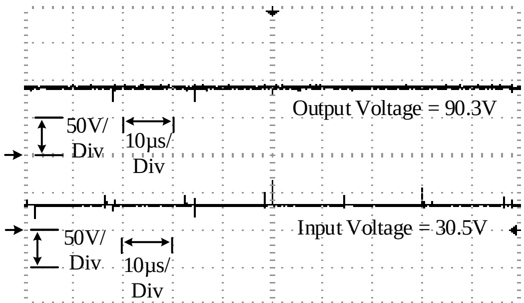


(b) Experimental

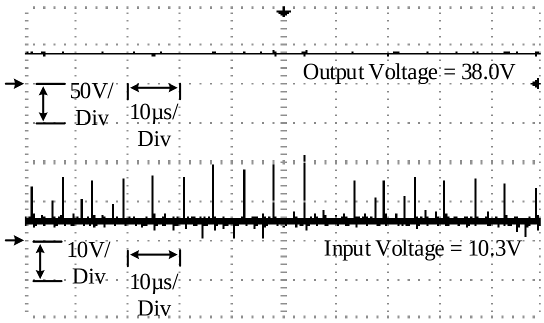
Fig. 7 - Switching signal with dead time



(a) One-stage IMMCC



(b) Two-stage IMMCC

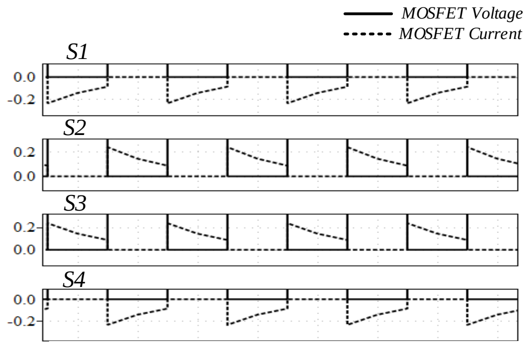


(c) Three-stage IMMCC

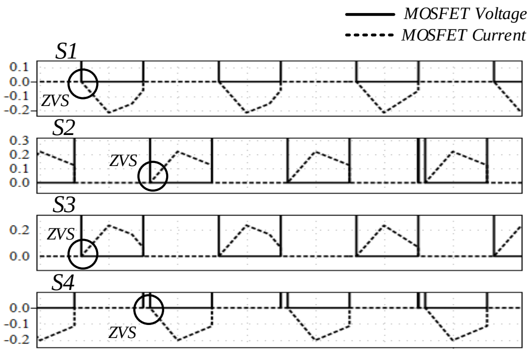
Fig. 8 - Experimental results of the input and output voltages

4.3 Resonant IMMCCC Simulation Result

For the resonant IMMCCC, soft-switching condition is achieved during turn-on and it considers zero voltage switching (ZVS). The ZVS is occurred at all switching devices. Figs. 9(a) and 9(b) show the hard-switching and soft-switching conditions for the IMMCCC and resonant IMMCCC, respectively. Only simulation work is conducted for the resonant IMMCCC in this is study.



(a) Hard-switching



(b) Soft-switching

Fig. 9 - IMMCC switching scheme

5. Switching loss and Voltage Stress

For the IMMCCC circuit, the increasing number of stages cause increasing the switching devices. Thus, switching loss becomes higher if number of stages are increased. Estimation of the switching loss is based on Equation (6), Equation (7) and Equation (8). The estimation of rise time, T_r and fall time, T_f refers on the datasheet of the switching devices. Fig. 10 shows the relationship of switching loss and number of stages. Besides, voltage stress of the switching devices is reduced when the number of stages is increased. Meanwhile, Fig. 11 shows the relationship between voltage stress and number of stages. It is obvious that, voltage stress of the conventional DC-DC boost converter is higher as compared to the IMMCCC with fixed output voltage.

$$W_{sw(on)} = \frac{1}{6} V_{DS} I_{DS} (t_r + t_{d(on)}) \tag{6}$$

$$W_{sw(off)} = \frac{1}{6} V_{DS} I_{DS} (t_f + t_{d(off)}) \tag{7}$$

$$P_{sw} = \left[W_{sw(on)} + W_{sw(off)} \right] \times f_{sw} \tag{8}$$

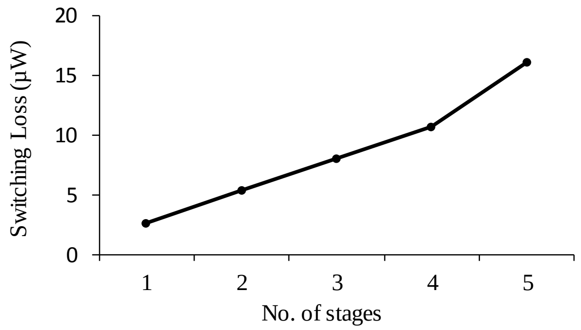


Fig. 10 Relationship switching loss and number of stages

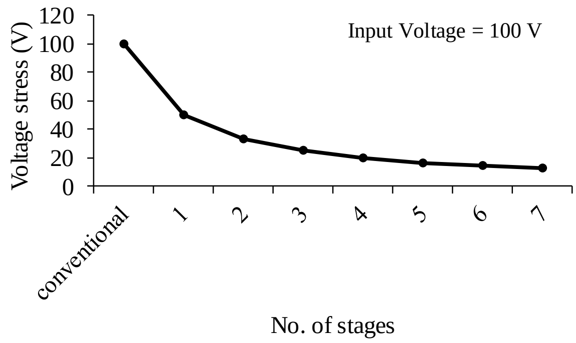


Fig. 11 - Relationship between voltage stress and number of stages

6. Conclusion

The study shows the IMMCCC structure has several advantages as compared to the conventional DC-DC converter, i.e., higher output voltage gain and lower voltage stress on semiconductor devices. Specifically, with the IMMCCC structure, high voltage gain can be achieved regardless of the duty cycle influence. Based on the experimental results, the obtained output voltages are 60 V (boost ratio 2), 90 V (boost ratio 3) and 120 V (boost ratio 4) with the input voltage of 30 V and fixed duty cycle of 50% for the one-stage, two-stage and three- stage of the IMMCCC structures, respectively. Meanwhile, for the conventional converter, the output voltage is always double when duty cycle is 50%. Since the structure is inductor less, size and volume of the converter can be optimized.

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