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A 2x2 Bit Multiplier Using Hybrid 13T Full Adder with Vedic Mathematics Method

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Abstract: Various arithmetic circuits such as multipliers require full adder (FA) as the main block for the circuit to operate. Speed and energy consumption become very vital in design consideration for a low power adder. In this paper, a 2x2 bit Vedic multiplier using hybrid full adder (HFA) with 13 transistors (13T) had been designed successfully. The design was simulated using Synopsys Custom Tools in General Purpose Design Kit (GPDK) 90 nm CMOS technology process. In this design, four AND gates and two hybrid FA (HFAs) are cascaded together and each HFA is constructed from three modules. The cascaded module is arranged in the Vedic mathematics algorithm. This algorithm satisfied the requirement of a fast multiplication operation because of the vertical and crosswise architecture from the Urdhva Triyakbyam Sutra which reduced the number of partial products compared to the conventional multiplication algorithm. With the combination of hybrid full adder and Vedic mathematics, a new combination of multiplier method with low power and low delay is produced. Performance parameters such as power consumption and delay were compared to some of the existing designs. With a 1V voltage supply, the average power consumption of the proposed multiplier was found to be 22.96 µW and a delay of 161 ps.

Keywords: Hybrid Full Adder, Pass Transistor, Multiplier, Low Power, High Speed

1 Introduction

Nowadays very large scale integration (VLSI) chips have led to rapid and innovative development in low power design. In recent years, the growth of personal computing devices such as portable computers and real time audio and video based multimedia applications, and wireless communication systems had made power dissipation a most critical design parameter. The need for low power design is also becoming a major issue in high performance digital systems such as microprocessor, digital signal processor and other applications. For these applications, multiplier is the major core block [1]. It functions as a fundamental operation in most signal processing.

A multiplier is a very important element in most of the processors and contributes substantially to the total power consumption of the system. Using complementary metal oxide semiconductor (CMOS) logic circuits for applications in various digital signal processors, and based on the multiplier method chosen for a particular processor, an efficient high speed, low power and small size integrated circuit (IC) can be designed [2].

There are many multiplication algorithms can be used to design the multiplier, for instance carry-select adder (CSA) and Wallace Tree method [3]. Each of these algorithms has its own advantages in terms of speed, power consumption, layout regularity and area. Although there are many multiplication algorithms, Vedic algorithm [4] claims to be the most interesting algorithms. It works based on the natural principles on which the human mind works.

Vedic mathematics propose simple approaches, towards the normal mathematical operations. The word "Vedic" is derived from the word "Veda" which means the store house of the knowledge. Vedic mathematics is the ancient methodology of the Indian mathematics. It has the unique technique of calculation based on the 16 sutras (formulae) [5]. It covers several modern mathematical terms including arithmetic, geometry, trigonometry, quadratic equations, factorization and even calculus. The implementation of the Vedic algorithm in the multiplier is based on the Urdhva Triyakbhyam Sutra [4] - [6] which is a general multiplication formula applicable to all cases of multiplication. This algorithm satisfied the requirement of a fast multiplication operation because of the vertical and crosswise architecture from the Urdhva Triyakbyam Sutra [7] which reduced the number of partial products compared to the conventional multiplication algorithm. By using the Vedic mathematics, a less number of steps are required for multiplication, thus the multiplier will be more power efficient, faster and small in size. It is one of the feasible techniques to be implemented in VLSI design to overcome the power dissipation issue as the number of transistors increased as stated in Moore's law.

2 Materials and Methods

The 2x2 multiplier circuit was designed by using four AND gates and two 13T hybrid full adders as shown in Figure 1. Four input voltages of 1V are used for input A1, A0, B1 and B0. The two 13T HFAs are drove by the output produced by AND gate. 13T HFA is chosen instead of half adder due to the specialty of 13T design.

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Each module in 13T HFA is designed individually so that it can be optimized in terms of power, delay and area.

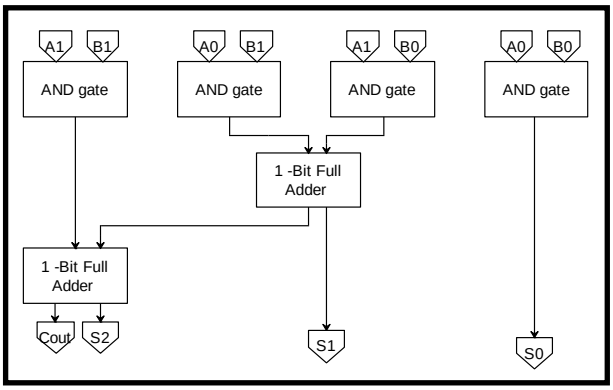

Figure 1 Block Diagram for 2x2 bit Vedic Multiplier

2.1 1-bit Hybrid Full Adder (HFA)

The 1-bit hybrid full adder (HFA) circuit was designed by constructing the full adder using three modules as shown in Figure 2 [8]. XOR circuit is inside Module I and with an inverter, a XOR-XNOR combination will be produced to drive the other two modules. The new sum circuit (SUM) is generated through Module II, and Module III generates carry signal (C_{OUT}). Both of the later modules rely on the output of the first module, thus Module I must have a good driving capability and should be able to produce a full swing output simultaneously.

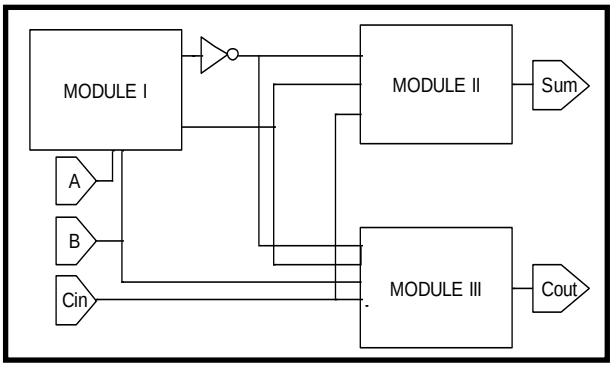

Figure 2 Block Diagram for Hybrid Full Adder

Module I is a XOR gate made up of only three transistors (3T). The design is based on a modified version of CMOS inverter and a PMOS pass transistor [9]. Module II is a new circuit being designed called unique sum circuit to produce output SUM for the HFA [8]. Only four transistors are used in this design as compared to the circuit designed by Suguna which used six transistors [10]. The input to this new sum circuit is coming from the carry-in bit (C¬in) along with the output of module I (XOR) and its inverted form (XNOR). XOR, XNOR and carry-in (Cin) are used to control the gate of the respective transmission gate in design. Meanwhile, the output (SUM) of this module depends on the output value of XOR and XNOR gates. The Module III consists of two sets of transmission gate which are controlled by XNOR and XOR. Either one of these transmission gates will allow the input signals (Cin or B) to propagate through. Output carry-out (C_{OUT}) is produced by this module.

2.2 Different Technique Used in Designing Multiplier

Table 1 shows different techniques which have been used in designing multiplier either using application specific integrated circuit (ASIC) method through Xilinx Integrated Synthesis Environment (ISE) or full custom design using Tanner EDA with PDK 180 nm.

Table 1 Techniques in Designing Multipliers

	Bits	Techniques	Delay (ns)	Power Consu-mption (W)	Techn -ology
[11]	8	Vedic mathematics	21.50	-	XilinxISE12.2i
[12]	8	Booth algorithm	30.45	-	Xilinx ISE 12.1
[12]	8	Modified booth algorithm	21.75	-	Xilinx ISE 12.1
[13]	8	Radix 4	27.11	15 x 10-3	Xilinx ISE 8.2i
[5]	8	Vedic mathematics	19	1.46 x 10-4	Tanner EDA
[14]	8	Positive Feedback Adiabatic Logic (PFAL)	-	4.53 x 10-4	Tanner EDA 180nm
[14]	8	Efficient Charge Recovery Logic (ECRL)	-	6.11 x 10-4	Tanner EDA 180nm
[15]	4	Wallace Tree	31.3	18.3 x 10-3	180nm CMOS Techn-ology

From previous research, many techniques had been used to design a multiplier, and one of them is the Booth multiplier [12]. Booth algorithm is the standard technique used in chip design which allowed for smaller and faster circuits. However, this conventional array multiplier required large silicon area. Larger silicon area is required in order to remove the heat generated due to large power consumption causes by complex logic [16], thus it had a high delay time. Another common technique is Wallace tree. It was implemented by Chris Wallace. Wallace tree has a complex circuit [3] which lead to the usage of larger

area. In [15], Wallace tree multiplier with only 4 bit is reported having high power consumption and long delay. Another multiplier, Radix 4 reduced the delay; but the main drawbacks are high cost and low utilization [17]. Positive feedback adiabatic logic (PFAL) and efficient charge recovery logic (ECRL) are types of adiabatic logic circuit [14] which have simple architecture and power clock system. In ECRL, coupling effects happened due to the interfere of outputs toward the PMOS latch. This problem had been overcame by PFAL thus the power consumption of PFAL is lower than ECRL [18]. Vedic mathematics is another method that can be used in designing multiplier. According to [11] and [5], Vedic mathematics multiplier shows it has a good performance in delay time and power consumption both in ASIC and full custom design. The implementation of the Vedic algorithm in the multiplier is based on the Urdhva Triyakbhyam and this algorithm satisfied the requirement of a fast multiplication operation because of the vertically and crosswise multiplication concept [19].

Different CMOS technology and design method had been used to design a multiplier. The delay and total power consumption estimation can be varied which depends on various parameter [20]. Although the techniques in Table 1 cannot be compared one to one due to different technologies and methods, the table merely shows that designing a multiplier using Vedic mathematics is the wise choice according to the results shown in [11] and [5].

2.3 Vedic Mathematics - Urdhva Triyakbhyam Sutra

The Vedic multiplier is based on Urdhva Tiryakbhyam Sutra, which is one of the ancient Indians mathematics. It is known as a general multiplication formula applicable to all cases of multiplication. It literally means "vertical and crosswise". This formula is generalized for n x n bit numbers [5]. Urdhva Tiryakbhyam Sutra Vedic algorithm satisfied the requirement of a fast multiplication operation because of the vertically and crosswise multiplication concept [19] that adapted well to parallel multiplication process. Hence, it greatly reduced the number of partial products leading to fast multiplication process. To further explain the multiplication pattern, A1, A0, B1 and B0 is used in Figure 3 to illustrate multiplication process.

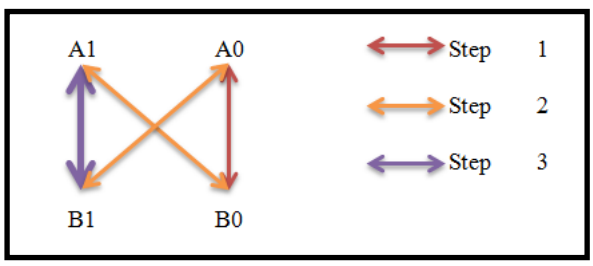

Figure 3 Multiplication of 2x2 bit Vedic Multiplier

Initially, the process takes into account the vertical multiplication of least significant bit (LSB), A0 and B0, giving a product of P0. Afterwards, the LSB of multiplicand is multiplied by the subsequent higher digit of multiplier followed by the addition of outcome. Cross multiplication of A1·B0 and A0·B1 happened. The partial products produced from the cross multiplication are summed up to give a product of P1 and a carry, C0. Lastly, vertical multiplication of most significant bit (MSB). The partial product produced is then summed up with the carry, C1 from step 2 resulting product of P2. Product P2 is the carry, C1, from the addition of partial product A1·B1 and carries C0.

$$S0 = A0*B0 \quad (1)$$

$$C1S1 = (A1*B0) + (A0*B1) \quad (2)$$

$$C2S2 = C1 + (A1*B1) \quad (3)$$

Based on these equations, the end result is C2P2P1P0. Similarly, the other cases can be computed. In similar method, a 4, 8 and N bit multiplier can de designed with little modification [11].

2.4 2x2 Bit Multiplier using Vedic Mathematics

The 2×2 bit Vedic multiplier module is implemented using four input AND gates along with two full adders. The design was simulated using General Purpose Design Kit (GPDK) of Synopsys Custom Tools using 90 nm CMOS technology process. 2×2 bit Vedic multiplier design starts by designing and simulating different gates separately using Custom Designer Schematic Editor jointly with Hspice to visually assemble the circuit schematic and simulation works is done to verify the gates. Output waveform can be viewed in WaveView. After a correct result is obtained, a symbol is created for the particular schematics and it is cascaded with other circuits to form a complete 2×2 bit Vedic multiplier module which is shown in Figure 4. The tested output waveform in Figure 5 is correct as it is similar to the truth table in Table 2.

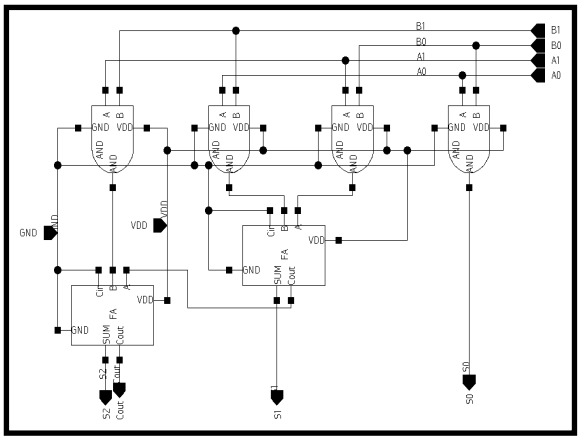

Figure 4 Schematic Diagram for 2x2 Bit Multiplier

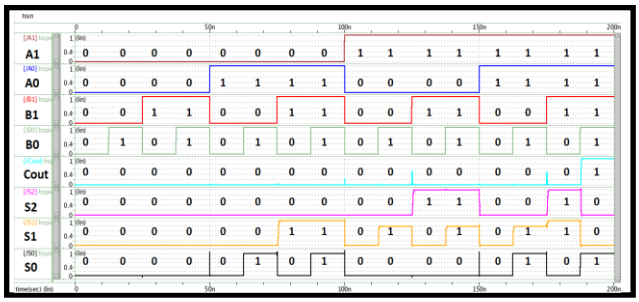

Figure 5 Output Waveform for 2x2 Bit Multiplier

Table 2 Truth Table of 2x2 Bit Vedic Multiplier

INPUT				OUTPUT			
A1	**A0**	**B1**	**B0**	**COUT**	**S2**	**S1**	**S0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

In this project, the design of a low power and high speed Vedic multiplier using hybrid pass transistor logic (PTL) and new SUM circuit is carried out. A hybrid PTL and new SUM circuit are realised with complementary metal-oxide-semiconductor (CMOS) technology. The concept is implemented to design full adders and multipliers

3 Results and Discussion

3.1 Delay in 1-bit Full Adder

The propagation delay of the proposed circuit is shown in Table 3 along with several other 1-bit full adders which have been designed using power supply of 1 V to 1.8 V. This table is arranged from the highest number to the lowest number of transistors used in each of the 1-bit full adder. The proposed 13T hybrid full adder is able to produce a delay of 104 ps and this is achievable using 90 nm CMOS technology with only 1 V power supply. This is a significant achievement since a faster circuit can be obtained by using smaller technology without compromising the circuit functionality. The result shown that the proposed HFA is able to perform 70.28% faster than the original design in [8]. Both of these designs using the same algorithm and number of transistors counts, but these designs are different in the GPDK used and the power supply.

The 1-bit full adder in this project also has a better performance in delay when compared to other design. The 28 transistors (28T) full adder in [21] had used GPDK 32 nm that has robustness against voltage scaling and transistor sizing, but the proposed HFA performs a 57.20% less delay than the 28T full adder. This is because the 28T full adder requires buffer during the operation thus creating high capacitance and bigger area compared to the proposed 13T HFA. The HFA used in this project is able to perform about 90.7% faster than the 20 transistors (20T) full adder in [22]. Also when compared to a hybrid full adder which uses 16 transistors (16T) with GPDK of 180 nm [23], the 13T HFA in this project is able to produce an output with less delay.

Table 3 Delay in Different Full Adder

	Power supply (V)	**Transistor (T)**	**Delay (ps)**	**CMOS Technology**
This project	1	13	104	HSPICE-90nm CMOS Technology
[21]	1	28	243	Tanner EDA- 32nm CMOS Technology
[22]	1	20 (GDI + MUX)	1120	SPICE-90nm CMOS Technology
[22]	1	20 (Hybrid)	1116	SPICE-90nm CMOS Technology
[23]	1.8	16 (Hybrid)	224	Cadence-180nm CMOS Technology
[8]	1.8	13	350	Tanner EDA-250nm CMOS Technology
[24]	1.2	8	185900	HISPICE-180nm CMOS technology
[24]	1.2	6	200124	HISPICE-180nm CMOS technology

It is reported that 8 transistors full adder and 6 transistors can be designed using deep submicron technology [24]. These full adders acquire the least area

among all other 1-bit full adder designs but they produce a high delay due to the usage of transmission gate. Besides, the 6 transistors full adder is not able to produce output with a full swing waveform [25] and this type of full adder will suffer when cascading is done to form higher bits adder and the result of the final output will be affected. Thus overall it can be said that the HFA that used in this project is able to provide an output with a least delay among others.

3.2 Comparison of Power Consumption for 1-bit Full Adders

The average power consumption of the proposed 13T HFA is 44.64 µW. The power consumed by the proposed 13T HFA is higher than most of the designs as shown in Table 4 accept when compared to the full adder in [26]. The proposed 13T HFA consumed 61.68% less power than the work reported in [26]. Thus further modification and analysis will be made to the proposed HFA in order to lower the power consumption.

Table 4 Comparison of Power Consumption in Different Full Adders

	Power supply (V)	Transistor (T)	Power Consu-mption (µW)	CMOS Technology
This project	1	13	44.64	HSPICE-90nm CMOS Technology
[21]	1	28	4.56	Tanner EDA 32nm CMOS
[22]	1	20 (GDI + MUX)	4.36	SPICE 90 nm CMOS
[22]	1	20 (Hybrid)	8.45	SPICE 90 nm CMOS
[23]	1.8	16 (Hybrid)	4.16	Cadence Virtuoso 180 nm CMOS
[8]	1.8	13	2.09	Tanner EDA 250 nm CMOS
[26]	1.8	8	116.5	Cadence Virtuoso 180 nm CMOS

3.3 Vedic Mathematics Techniques Used in Multiplier

A review and comparison of various kind of Vedic mathematics method used in multiplier is shown in Table 5. Vedic mathematics is very useful in its own right but it can be more effective when combined with other techniques where they can facilitate different structures to achieve low power or even high speed circuit.

Table 5 Different Types of Vedic Mathematics Method Used In Multiplier

	Techniques	Delay (ns)	Power Consump-tion(W)	Techno-logy
[27]	Vedic mathematics + adiabatic efficient charge–recovery logic (ECRL) (8)	4.750	4.642	Tanner EDA
[28]	Vedic mathematics + fast adder	1.040	0.358	Synopsys Design Compiler (65nm)
This project	Vedic Mathematics + 13T HFA	0.161	22.96 x10-3	HSPICE-90nm CMOS Technology

By comparing the delay time of different techniques that work together with Vedic mathematics, the proposed 2x2 multiplier with 13T HFA is able to produce a reasonable delay which is 22.96 µW. The power consumption of the 2x2 multiplier is less than the other two circuits. Thus the combination of Vedic mathematics and 13T HFA in the 2x2 multiplier which had been used in this project, can be considered a good circuit with a low power consumption. However it should be noted that the technology and power supply of the compared circuits are different.

4 Conclusion

In this paper, a 2x2 bit Vedic multiplier using 1 bit hybrid full adder with 13 transistors (1-bit 13T HFA) is proposed. The design was simulated using Synopsys Custom Tools in General Purpose Design Kit (GPDK) 90 nm CMOS technology process. The 2x2 bit Vedic multiplier is performing well in terms of delay and power consumption as compared to other reported 2x2 multipliers. The proposed 2x2 bit Vedic Multiplier consumed the least power consumption (22.96 µW at 1V). It also has a shortest delay of 104ps, and can produce undistorted output with a full swing. Only 50 transistors are used and the area for the layout is considered small. The proposed 2x2 Bit Vedic Multiplier with 1-bit hybrid full adder circuit has a special sum circuit (module II) by using only 4 transistors. The 1-bit full adder is called hybrid since it mixes the concept of pass transistor and transmission gates along with the regular fully complementary inverter and 3 transistors XOR gate (module I).

The 1-bit 13T HFA design and 2x2 bit Vedic multiplier will be further used to form 8-bit full adder and later will be implemented in 8x8 bit multiplier.

Modification in transistors level will be made in future in order to achieve better performance

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