IJIE

INTERNATIONAL JOURNAL OF INTEGRATED ENGINEERING
ISSN: 2229-838X e-ISSN: 2600-7916

Vol. 18 No. 3 (2026) 327-339
https://publisher.uthm.edu.my/ojs/index.php/ijie

Enhancing Harmonics Mitigation of 5-Level Cascaded H-Bridge Inverter Through Fuzzy Proportional Voltage Balancing Control

Swee Xiang Yong, Yap Hoon[1]*, Hou Kit Mun[1], Foo Wah Low[1]

[1] *Lee Kong Chian Faculty of Engineering and Science,*
Universiti Tunku Abdul Rahman, Kajang 43000, Selangor, MALAYSIA

*Corresponding Author: hoonyap@utar.edu.my
DOI: https://doi.org/10.30880/ijie.2026.18.03.022

Article Info

Received: 29 July 2025
Accepted: 4 March 2026
Available online: 30 April 2026

Keywords

Shunt Active Power Filter (SAPF), harmonics, DC-link voltage unbalance, cascaded H-Bridge (CHB)

Abstract

This work presents a novel approach to enhancing harmonics mitigation in 5-level cascaded H-Bridge inverter (5-lv CHB) through a Fuzzy Proportional Voltage Balancing Control technique. The proposed technique is applied to a Shunt Active Power Filter (SAPF) system to effectively reduce Total Harmonic Distortion (THD) in power systems. By dynamically balancing the voltages of the inverter's DC-link capacitors, the proposed technique minimizes overshoot and ripple in the output waveform, ensuring a more stable and efficient operation. Simulation results demonstrate that the proposed technique significantly outperforms traditional voltage balancing technique, achieving improved harmonic suppression and reduced THD under varying load conditions. This approach provides a robust solution for enhancing power quality in modern power systems.

1. Introduction

The global shift towards sustainable energy has necessitated the integration of renewable sources into Malaysia's distributed generation systems. As this trend accelerates, ensuring effective power quality management is essential for seamless grid interaction. One predominant issue is harmonic distortion, which can severely degrade system performance. The SAPF has emerged as a critical technology for addressing these challenges, effectively mitigating harmonic distortions [1].

The SAPF operates by injecting compensating currents into the grid to eliminate harmonic currents and reactive power caused by non-linear loads. In recent years, multilevel inverter-based active power filter (MI-APF) have garnered significant attention for their superior ability to enhance power quality and efficiency compared to traditional SAPF that utilize two-level inverters. Traditional SAPF are prone to high switching losses and increased risk of switch failure, making MI-APF a more reliable and efficient alternative. Hence, MI-APF has become a reliable and efficient method instead of 2-level inverter based APF. Moreover, MI-APF also can eliminates the need for passive filter, bulky transformer, and lower the switching loss and stress of switches [2–4].

Furthermore, multilevel inverter has three common topologies, like diode-clamped multilevel inverter, flying capacitor multilevel inverter and CHB multilevel inverter. A comparison of multilevel inverter topologies indicates that the CHB inverter is preferable due to its modular structure and reduced component count. Hence, CHB multilevel inverter can decrease the switching frequency and easier to scale up for higher voltage and power levels due to its modular design [5–7]. However, CHB inverter has a serious problem which is voltage imbalance. This issue prevents the CHB multilevel inverter from achieving optimal performance. The reason of this voltage imbalance

This is an open access article under the CC BY-NC-SA 4.0 license.

issue is the switching sequence for each H-bridge cell is different, so it causes the charge and discharge rates of the DC-link capacitors unequal. As a result, the performance and reliability of the SAPF can be compromised, so a robust voltage balancing algorithms emerges as a promising solution [8].

Typically, voltage balancing control needs two types of algorithms which are feedback control algorithms and switching control algorithms. Feedback control algorithms is to decrease the voltages error between the DC-link capacitors and then the switching control algorithm is to control the power switches of multilevel inverter to achieve voltage balancing. Normally, feedback control and switching control algorithms need to work together to get the optimal performance.

For the feedback control, the most common and general technique is proportional-integral (PI) control due to its simplicity and performance. However, the performance of a PI controller may fall short in voltage balancing algorithms, primarily due to intrinsic response delays, particularly when managing non-linear loads [9].

Furthermore, switching control algorithms are crucial for voltage balancing as they manage the timing and sequence of switching actions to regulate the system's output voltage, current, and overall performance. A widely used technique for managing many power switches is multicarrier sinusoidal PWM (MCSPWM). This algorithm involves comparing multiple carrier signals with a reference sinusoidal waveform to produce the required switching pulses for each power switch. The carriers are arranged in different configurations, such as phase disposition PWM (PDPWM), phase opposition disposition PWM (PODPWM), alternative phase opposition disposition PWM (APODPWM), quarterly fundamental cycle rotation PWM (QRPWM) and more, depending on the desired output waveform characteristics and harmonic performance. Although alternative MCSPWM algorithms have been effectively utilized to manage the basic operation of CHB inverters, research remains limited on their performance when applied to control CHB inverters as SAPF. In such applications, the control processes become significantly more complex due to the need to mitigate harmonics present in the power system [10–12].

As FLC technology develops, the integration of FLC into voltage balancing algorithms has become a reliable solution for this voltage imbalance issue and the problems faced by existing techniques. This is because FLC can provide robust and adaptive control capabilities, making it highly suitable for managing the challenges of power system dynamics and non-linear loads [9,13,14].

This research seeks to explore and tackle the challenges related to the implementation of SAPF, especially concerning voltage imbalance in 5-lv CHB inverters. This work proposes an FLC-based voltage balancing algorithm to solve the problem of unequal DC-link voltages in CHB inverters. By integrating FLC into the voltage balancing technique, the primary scope of this work is to improve the overall performance and reliability of the MI-APF for power quality problems mitigation. The effectiveness of the proposed technique is evaluated through a comprehensive test environment using MATLAB/Simulink. Simulations are conducted under distorted supply, with both capacitive (RC) and inductive (RL) non-linear loads. The performance is analyzed during steady-state and dynamic-state conditions, and a comparative analysis is carried out against an existing benchmark technique to ensure that the proposed technique delivers superior results for optimal SAPF operation.

2. Research Design

In this work, a 5-lv CHB inverter as shown in Figure 1 is employed as it provides an optimal balance between complexity and performance [15,16]. Figure 1 shows the schematic diagram and the output voltages (V_{AN}, V_{A0}, V_{0N}) of 5-lv CHB inverter. Figure 1 also illustrates the structure of the 5-lv CHB inverter, consisting of two H-bridge cells: an upper cell (H1) and a lower cell (H2).

Int. Journal of Integrated Engineering Vol. 18 No. 3 (2026) p. 327-339

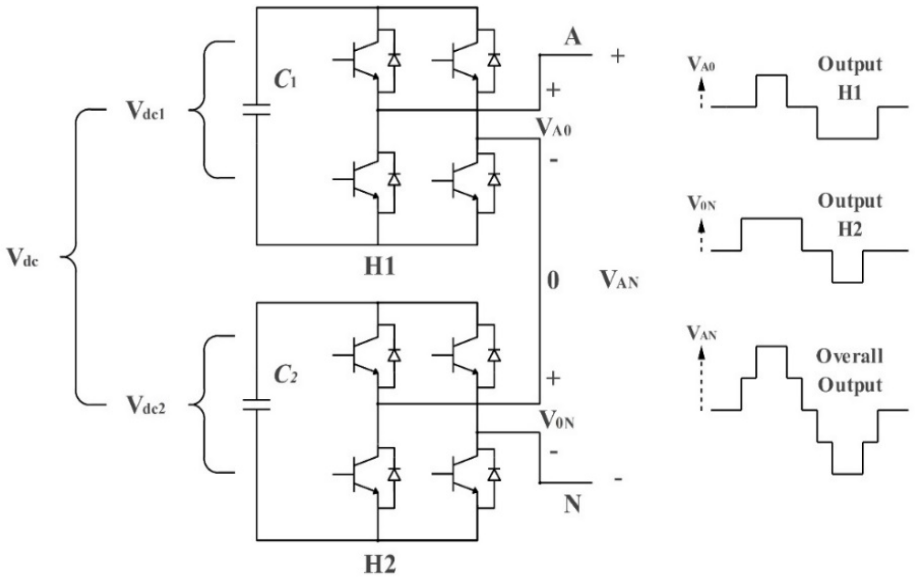
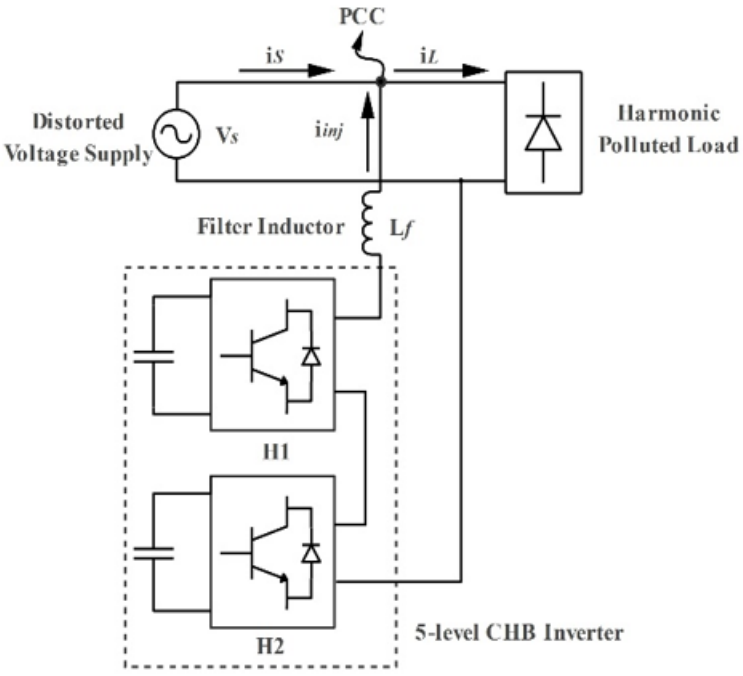
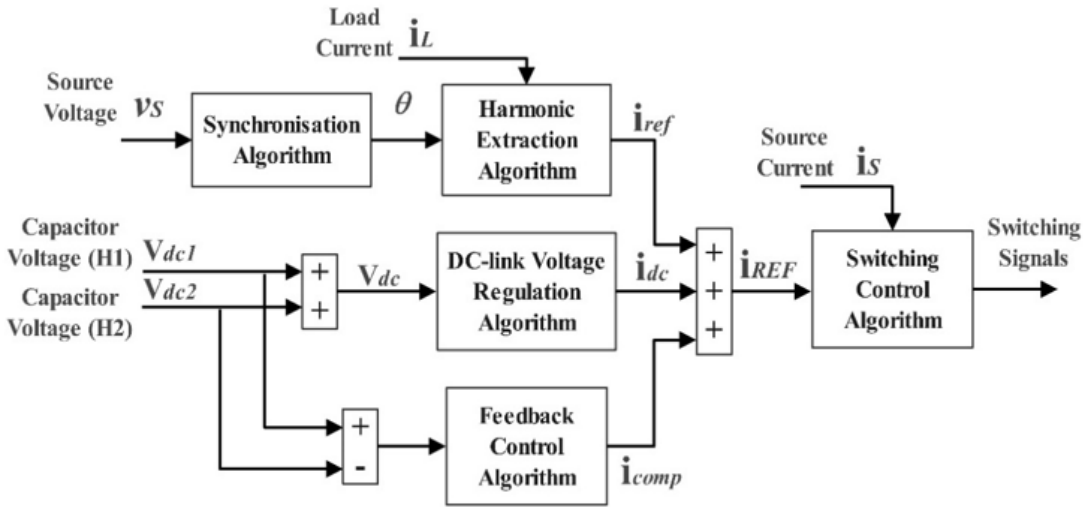


Fig. 1 *5-lv CHB inverter and output voltage waveforms*

To develop a fully functional 5-lv CHB Inverter APF, several additional algorithms are required beyond just feedback and switching control. These include synchronization algorithm to align the inverter's output with the grid, harmonic extraction algorithm to accurately identify and isolate unwanted harmonics, and voltage regulation algorithm to maintain stable overall DC-link voltage of the multilevel inverter. Each component is essential for ensuring the MI-APF operates efficiently and reliably in addressing power quality issues. Figure 2 shows the overview of control system of 5-lv CHB inverter based SAPF.



(a)



(b)

Fig. 2 *(a) Overview of control system; and (b) Algorithms applied for 5-lv CHB inverter based SAPF*

As presented in Figure 2, the SAPF is connected to the point of common coupling (PCC) to facilitate the injection current I_{inj} into the operating system to mitigate the harmonic current. The synchronization algorithm plays a key role in this process by accurately tracking the angular position of the source voltage signal (V_s). This tracking allows the calculation of the phase angle (θ), which is used to align the reference current (I_{ref}) from harmonic extraction with the phase of V_s. This alignment ensures that the SAPF interacts effectively with the power system, optimizing the harmonic compensation process [1].

The harmonic extraction algorithm identifies and separates the fundamental current from the harmonic currents. Using these characteristics, it generates a reference current (I_{ref}), which is derived alongside signals from the DC-link voltage regulation algorithm and feedback control (I_{dc}, i_{comp}). The resulting reference current (I_{REF}) is then passed to the switching control algorithm for further processing [17].

The DC-link voltage regulation algorithm ensures that the voltage across the DC-link capacitors (V_{dc}) remains at the desired level by controlling their charging and discharging processes. It compares the actual V_{dc} with its target value and generates a signal current (I_{dc}). This current is sent to create I_{REF}, which controls the charging or discharging of the capacitors. This step helps maintain the system's stability and performance [18].

The feedback control algorithm ensures that the voltages across individual DC-link capacitors within each H-bridge cell (V_{dc1}, V_{dc2}) are equal. Ideally, V_{dc1} and V_{dc2} should be identical. The algorithm compares the two voltages, generating a signal current (i_{comp}), which is used to create I_{REF}. This reference current helps control the charging and discharging of the capacitors, contributing to system stability and balance.

Moreover, the switching control algorithm uses I_{REF} to generate switching signals for the CHB inverter. These signals control the on/off states of the switches in the inverter, allowing it to produce the desired injection current. By carefully managing the switching actions, the 5-lv CHB inverter generates injection currents that effectively reduce harmonics and improve system performance.

Finally, this work emphasizes the importance of the voltage balancing algorithm, making the feedback control and switching control algorithms critical components of the system. These algorithms play an important role in maintaining stable and balanced DC-link voltages, ensuring the effective operation of the 5-lv CHB inverter. By enhancing these control strategies, the overall performance and reliability of the voltage balancing process are significantly improved.

3. Voltage Balancing Technique

This section will introduce the benchmark voltage balancing technique and the proposed voltage balancing technique and shows the difference between them. Subsequently, with reference to benchmark technique, the improvements that lead to the development of the proposed technique will be highlighted.

3.1 Voltage Imbalance Issue in 5-lv CHB inverter

Understanding the causes for individual DC-link voltage imbalances is essential to properly tackle the issue. These imbalances are due to differences in the control signals that activate power switches. These mismatch causes different switching pattern of the switches, which failed to charge or discharge the DC-link capacitors of the

Int. Journal of Integrated Engineering Vol. 18 No. 3 (2026) p. 327-339

inverter in an even manner. As shown in Figure 3a, the output voltages of H1 and H2 are unequal. Specifically, the output voltage of H1 slightly exceeds the range of 200V to -200V, while the output voltage of H2 falls slightly below this range. This results in an improper voltage balance between H1 and H2 of the 5-lv CHB inverter. After that, Figure 3b shows the voltage waveforms of overall DC-link voltage $\boldsymbol{V_{dc}}$, individual DC-link voltages $\boldsymbol{V_{dc1}}$, $\boldsymbol{V_{dc2}}$ and the voltage deviation $\Delta \boldsymbol{V}$ ($\boldsymbol{V_{dc1}}$_$\boldsymbol{V_{dc2}}$) without voltage balancing. From Figure 3b, the overall DC-link voltage still reaches its operating level, although the individual voltage $\boldsymbol{V_{dc1}}$, $\boldsymbol{V_{dc2}}$ cannot balance against each other without voltage balancing technique. Hence, a reliable and effective voltage balancing technique is needed to solve the voltage imbalance issue.

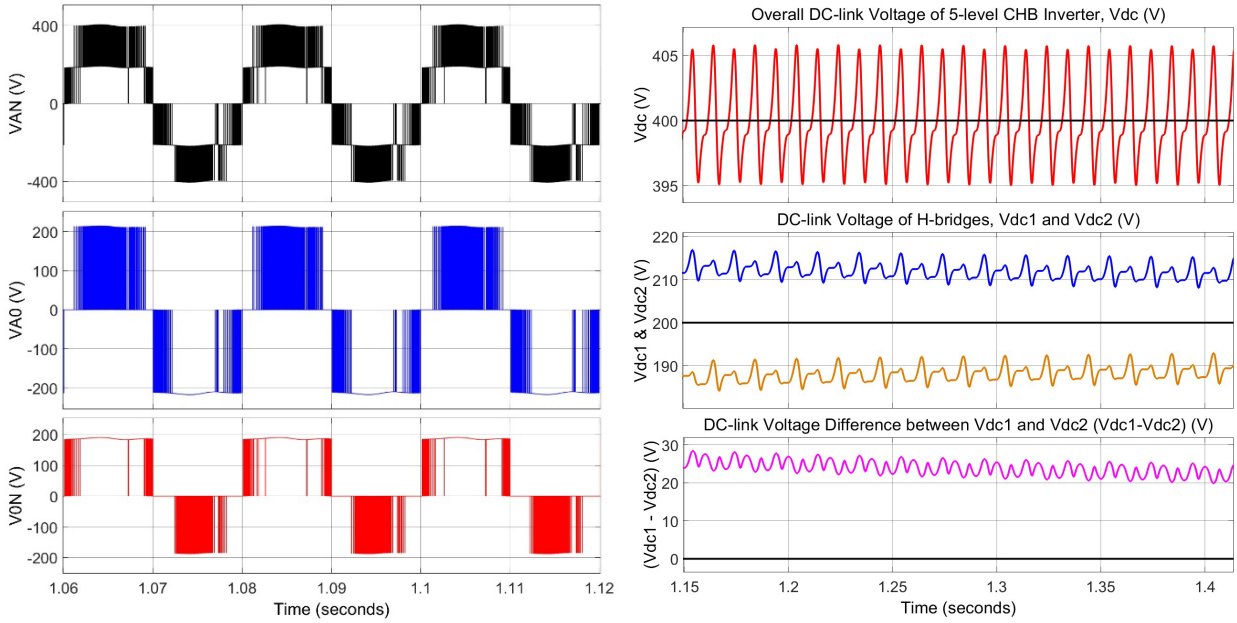


Fig. 3 *(a) Output voltage; and (b) DC-link voltage of 5-lv CHB inverter*

3.2 Benchmark Voltage Balancing Technique

QRPWM is the benchmark technique in this work which is a specialized modulation technique designed to enhance the performance of multilevel inverters. It operates by segmenting the fundamental cycle of the reference waveform into four equal quarters and rotating the carrier signals accordingly. This approach aims to improve harmonic performance, reduce switching losses, and achieve better voltage balancing in multilevel inverter systems [18,19].

QRPWM was selected as the benchmark technique in this study because it represents an advanced and well-established multicarrier modulation method that provides high-quality harmonic performance and improved voltage utilization compared to other traditional PWM schemes. Unlike conventional PWM algorithms, which often rely on fixed carrier arrangements, QRPWM introduces a dynamic carrier rotation mechanism. This rotation redistributes the switching activities across the inverter's power devices, resulting in a more uniform and reduced stress on individual switches. Additionally, the algorithm provides superior control over harmonic content, particularly in applications requiring high power quality, such as renewable energy systems, active power filters, and motor drives. These characteristics make QRPWM an effective reference for evaluating new control strategies that aim to improve voltage balancing and harmonic mitigation. Figure 4 below illustrates the configuration of reference and carrier signals for PDPWM and QRPWM, highlighting the differences between QRPWM and the more commonly used PDPWM.

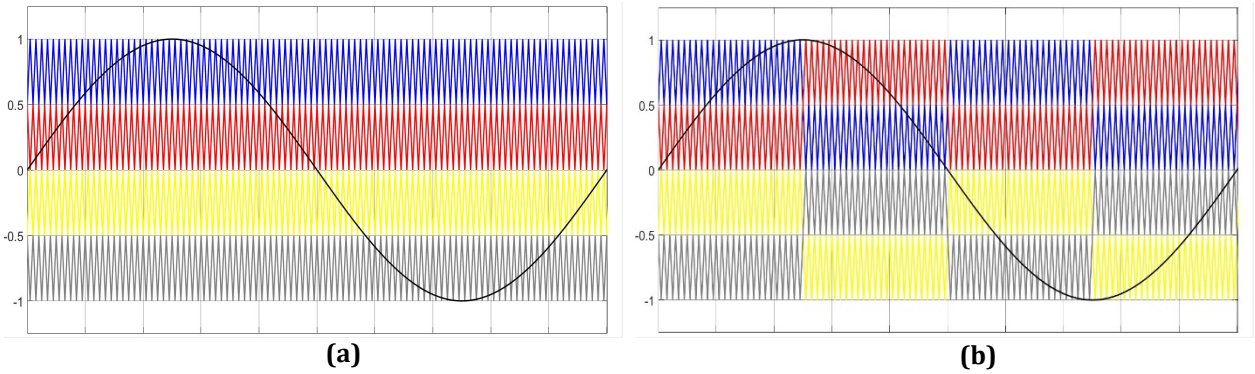


Fig. 4 *Configuration of (a) PDPWM; and (b) QRPWM*

While QRPWM offers numerous advantages, it also presents certain challenges that require careful consideration. A key issue is the increased complexity of the modulation scheme. The dynamic rotation of carriers demands more advanced control algorithms and greater computational resources compared to traditional PWM algorithms. During the vertical swapping of carrier signals at each quarter cycle of the reference signal, extra unnecessary vertical signals are generated at each exchange point. These signals are not part of the original triangular carriers, and their intersection with the sinusoidal reference signal can lead to unnecessary switching pulses. To implement this algorithm effectively, it is crucial to understand the interaction between the reference signal and each carrier signal. However, this becomes more challenging when dealing with many carrier signals, as required for operating multilevel inverters [20].

3.3 Proposed Voltage Balancing Technique

While the benchmark analysis highlights that QRPWM can deliver higher performance compared to other conventional PWM algorithms, its implementation significantly increases the system's complexity and operational challenges. To address this, a new voltage balancing technique is utilized instead of QRPWM.

For switching control algorithm, PDPWM is a widely adopted and straightforward switching control technique for multilevel inverters. In this algorithm, all carrier signals are aligned in phase, with their amplitudes vertically shifted to cover the inverter's DC bus voltage range. The sinusoidal reference signal is then compared with these carriers to generate switching pulses for the inverter's power devices. This simple structure makes PDPWM easier to implement and manage, reducing the system's computational and control requirements. However, PDPWM is not well-suited for handling non-linear loads, as it can lead to reduced effectiveness in system performance. To address this limitation and enhance PDPWM's effectiveness, improvements must be implemented in the feedback control algorithms.

For feedback control algorithm, the PI controller is the most used feedback control technique, it suffers from inherent limitations, particularly when handling non-linear loads. These limitations include time delays, higher THD, and slower system response. To address these issues, this work proposes the use of Fuzzy Proportional Control (Fuzzy-P), a type of FLC, to enhance feedback control performance.

Fuzzy-P combines the simplicity of traditional proportional (P) controllers with the flexibility and adaptability of fuzzy logic. It is designed to handle the limitations of conventional P controllers, particularly in systems with non-linearities, uncertainties, or varying operating conditions. Previous research has explored Fuzzy-P for nonlinear plant systems [21]. This concept is extended in the present study to the voltage balancing control of a five-level CHB inverter. Figure 5 shows the control structure of Fuzzy-P. Figure 5 shows the control structures of PI controller and Fuzzy-P controller.

In a standard P controller, the control action is directly proportional to the error signal. While effective in many linear systems, it can struggle in dynamic or complex systems where precise tuning and adaptability are required. Fuzzy-P addresses this limitation by replacing the fixed proportional gain with FLC that adjusts the control gain dynamically based on the system's current state.

The Fuzzy-P controller operates by regulating the voltage balancing of the multilevel inverter's DC-link capacitors. The controller is implemented using a Mamdani-type fuzzy inference system, which is well-suited for rule-based reasoning and interpretable control structures.

In this design, the controller uses a single-input, single-output structure. The input is the voltage deviation across the DC-link capacitors. The reason for selecting a one-input one-output scheme is to keep the controller simple and practical for real-time execution while maintaining sufficient effectiveness in correcting voltage imbalances. Since the rate of change of error is relatively slow for capacitor voltage in steady-state grid-connected systems, incorporating only the error as input is adequate to drive proportional corrective actions.

Int. Journal of Integrated Engineering Vol. 18 No. 3 (2026) p. 327-339

The fuzzy logic system uses five membership functions (MFs): Negative Big (NB), Negative Small (NS), Zero (ZE), Positive Small (PS), and Positive Big (PB). This five-level partition strikes a good trade-off between control resolution and design complexity. Fewer MFs could result in insufficient resolution and coarser control, while too many MFs would complicate the rule base without significant benefit for this application.

For the MF shapes, a combination of triangular and trapezoidal membership functions is selected. The triangular MFs are used for central linguistic terms (e.g., NS, ZE, PS) to provide a sharp and precise transition, while the trapezoidal MFs are applied at the extremes (NB and PB) to allow wider coverage of large deviations without sudden cut-offs. This arrangement ensures smooth inference transitions and avoids control discontinuities when the error shifts from extreme values back to moderate values. The rule base guiding the control logic includes:

1. If the voltage deviation is NB, then the output action is NB.
2. If the voltage deviation is NS, then the output action is NS.
3. If the voltage deviation is ZE, then the output action is ZE.
4. If the voltage deviation is PS, then the output action is PS.
5. If the voltage deviation is PB, then the output action is PB.

This dynamic, rule-based approach allows the FLC to adapt to varying load conditions in real-time, achieving smoother and more accurate control compared to traditional fixed-gain controllers. As a result, the system exhibits improved adaptability, reduced THD, and enhanced stability, making it highly effective in non-linear and dynamic power system environments.

For defuzzification, the Centroid of Area (COA) method is applied, which is a standard choice for Mamdani-type controllers due to its smooth and continuous defuzzied output. COA calculates the center of gravity of the aggregated fuzzy output set, ensuring that small variations in the input produce proportionate, predictable changes in the output. This property is vital to avoid abrupt switching or voltage oscillations.

The tuning of the Fuzzy-P controller was carried out iteratively in MATLAB/Simulink to achieve optimal performance. The initial membership function boundaries were determined based on the maximum observed capacitor voltage deviation during open-loop simulation. Further adjustments were made through repeated simulations under various load and supply conditions.

The main tuning objectives were to minimize the THD of the source current, reduce the DC-link voltage ripple, and ensure a fast transient response with minimal overshoot during dynamic load transitions. Performance was evaluated under both RC and RL nonlinear loads with distorted voltage supply. The membership function ranges, and output scaling factors were refined in successive iterations until the system achieved THD below 5%, a fast-settling time, and a significant reduction in voltage ripple.

After tuning, the Fuzzy-P controller exhibited strong adaptability and robustness, maintaining balanced DC-link voltages and superior harmonic mitigation compared with the conventional PI controller and the benchmark QRPWM technique. By combining the simplicity of PDPWM with the adaptability of the fuzzy controller, the proposed method achieves a practical balance between control complexity and performance.

Although QRPWM offers superior performance in some respects, the integration of FLC in this work compensates for the potential limitations of PDPWM. FLC significantly enhances voltage balancing and overall system performance, making PDPWM the more practical and effective choice in this setup. By leveraging FLC's robust control capabilities, PDPWM provides a balanced trade-off between simplicity and performance, ensuring reliable operation of the 5-lv CHB inverter as a SAPF. Besides that, QRPWM introduces additional vertical carrier signals during the swapping process, which can cause false switching pulses when the sinusoidal reference intersects with these unintended carriers. PDPWM avoids this issue by maintaining fixed carrier positions, resulting in more reliable switching behaviour. These improvements make the proposed voltage balancing technique a simpler, yet highly effective approach compared to the benchmark voltage balancing technique.

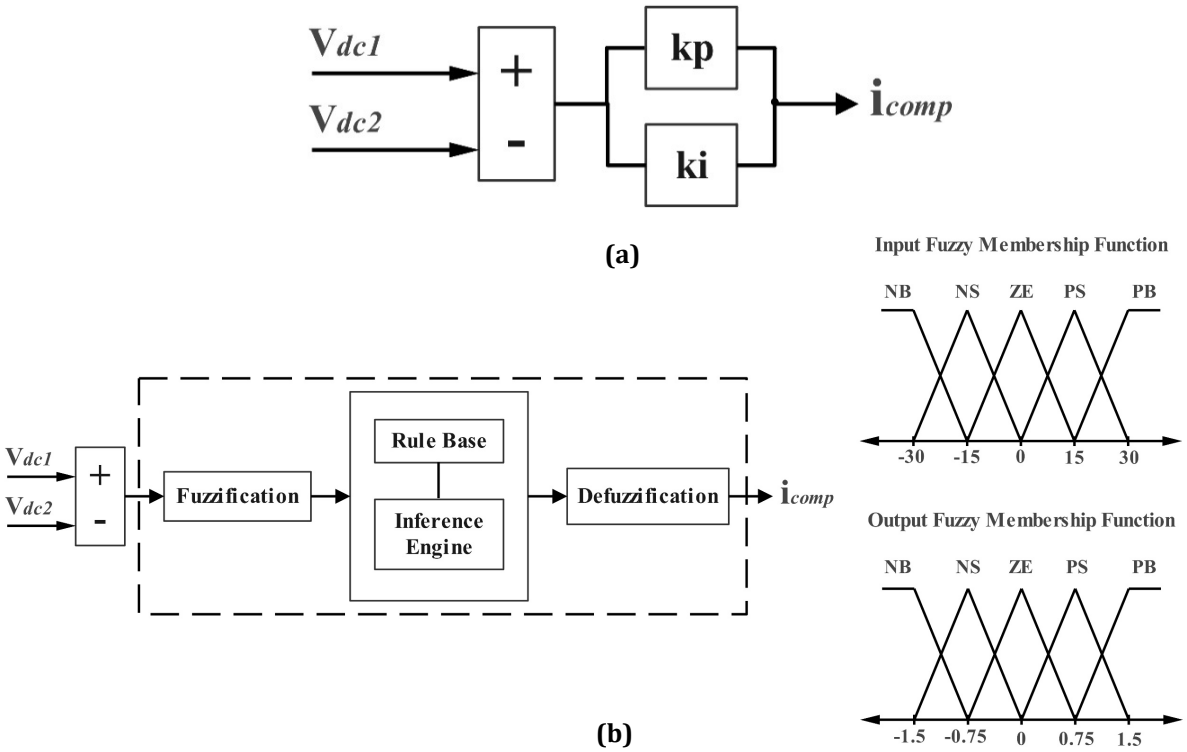


Fig. 5 *Control structure of (a) PI controller; and (b) The proposed Fuzzy-P controller*

4. Results and Discussion

The single-phase 5-lv CHB inverter-based SAPF, including benchmark and proposed voltage balancing techniques, is developed and tested in MATLAB/Simulink. The system's performance is assessed based on its ability to balance the DC-link voltages in the CHB inverter and minimize current harmonics within the power system. The evaluation is conducted under distorted supply conditions using two types of non-linear loads: capacitive (RC) and inductive (RL). Furthermore, the performance of the proposed voltage balancing technique is further evaluated under steady-state and dynamic-state conditions in terms of its ability to regulate DC voltages. A summary of all simulation parameters is provided in Table 1.

Table 1 *Simulation parameters of 5-lv CHB inverter*

Parameters	Values
Distorted Voltage Supply, V_s	Fundamental = 230V, 50Hz
(THD=17.09%)	3^{rd} Harmonic = 20V, 150Hz
	5^{rd} Harmonic = 10V, 250Hz
	7^{rd} Harmonic = 15V, 350Hz
	9^{rd} Harmonic = 5V, 450Hz
Overall DC-link Voltage, V_{dc}	400V
DC-link Capacitor, (C_1 & C_2)	3300 μF
RC load	50 Ω ; 470 μF
RL load	15 Ω ; 160 mH
Filter Inductance	3 mH
Switching frequency, f_s	5kHz
PI Controller	K_p = 0.8 K_i = 0.08

To comprehensively evaluate the performance of both the proposed and benchmark techniques, the model is tested under two conditions: steady-state and dynamic-state. Additionally, the output voltage waveform of the 5-lv CHB inverter is shown in Figure 6, demonstrating the generation of 5 level of voltages (-400 V, -200 V, 0 V, +200 V, +400 V) under RC and RL load conditions, as well as distorted supply conditions. These results validate the right

Int. Journal of Integrated Engineering Vol. 18 No. 3 (2026) p. 327-339

operation of the proposed technique as a 5-lv CHB inverter. Furthermore, Figure 6 also illustrates the output voltage waveforms of H1 and H2, each producing 3 levels of voltage (-200 V, 0 V, +200 V).

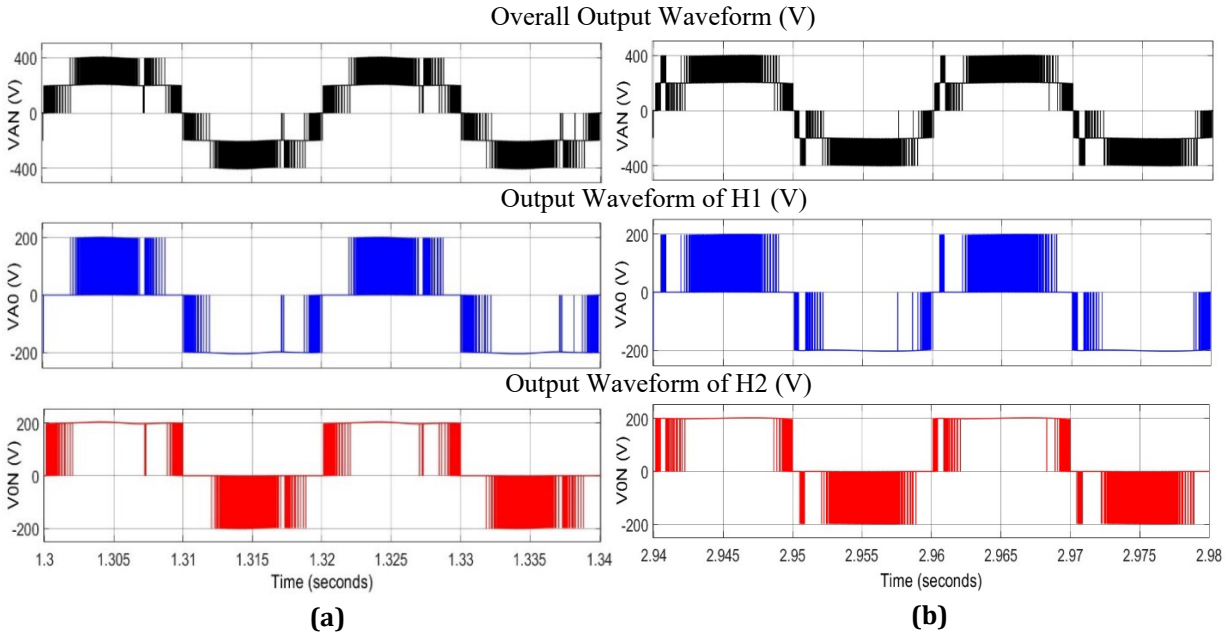


Fig. 6 *Output voltage waveforms of 5-lv CHB inverter demonstrated by the proposed technique for (a) RC; and (b) RL load conditions*

After that, Figure 7 shows the waveforms of voltage V_s, load current I_L, injection current I_{inj} and source current I_s of proposed techniques under RC and RL load conditions, as well as under distorted supply conditions. The results show that the injection currents generated by the CHB model, using both the proposed and benchmark techniques, effectively eliminate harmonics from load current. This harmonic mitigation of proposed and benchmark techniques produces a smoother sinusoidal waveform in the source current, which is also well-aligned with the phase of, V_s.

Additionally, Table 2 and 3 show the mitigation performance of proposed and benchmark techniques. The performance comparison of THD reduction for RC and RL loads highlights the effectiveness of the proposed voltage balancing technique. Without SAPF, the THD values are significantly high, reaching 112.22% for the RC load and 43.31% for the RL load. Using the benchmark technique, the THD values are reduced substantially to 3.28% and 1.82% for RC and RL loads, respectively. The proposed technique further improves these results, achieving THD reductions to 3.04% for the RC load and 1.74% for the RL load. This corresponds to an additional reduction of 7.3% for the RC load and 4.4% for the RL load compared to the benchmark technique, demonstrating the higher performance of the proposed technique in mitigating current harmonics. The phase difference results for RC and RL loads further validate the effectiveness of the proposed voltage balancing technique. Without SAPF, significant phase differences are observed, with 9.5° for the RC load and -7.9° for the RL load. The benchmark technique greatly minimizes these differences, reducing them to 0.5° for the RC load and -0.2° for the RL load. The proposed technique improves upon this performance, achieving phase differences of just 0.1° for the RC load and 0.0° for the RL load. These results highlight the better capability of the proposed technique in achieving higher phase alignment, enhancing the overall performance of the system.

Furthermore, Figure 8 and Table 4 show the peak-to-peak voltage ripple of overall DC-link voltage (V_{dc}), DC-link voltages of H1 and H2 (V_{dc1}, V_{dc2}), and DC-link voltage differences between H1 and H2 ($V_{dc1} - V_{dc2}$). Under steady-state conditions, for the RC load, the peak-to-peak voltage ripple is reduced from 7.0 V (3.5 to -3.5 V) using the benchmark technique to 5.2 V (2.6 to -2.6 V) with the proposed technique, representing a reduction of 25.7%. Similarly, for the RL load, the peak-to-peak voltage ripple decreases from 9.6 V (4.8 to -4.8 V) to 5.8 V (2.9 to -2.9 V), achieving a significant reduction of 39.6%.

Under dynamic-state conditions during a load change from RC to RL at 1.5 seconds, the peak-to-peak voltage ripple is reduced from 17.05 V (5.25 to -11.8 V) with the benchmark technique to 11.61 V (1.92 to -9.69 V) using the proposed technique, achieving a reduction of 31.9%. These results demonstrate the superior performance of the proposed technique in maintaining stable voltage levels across different load conditions and operating states.

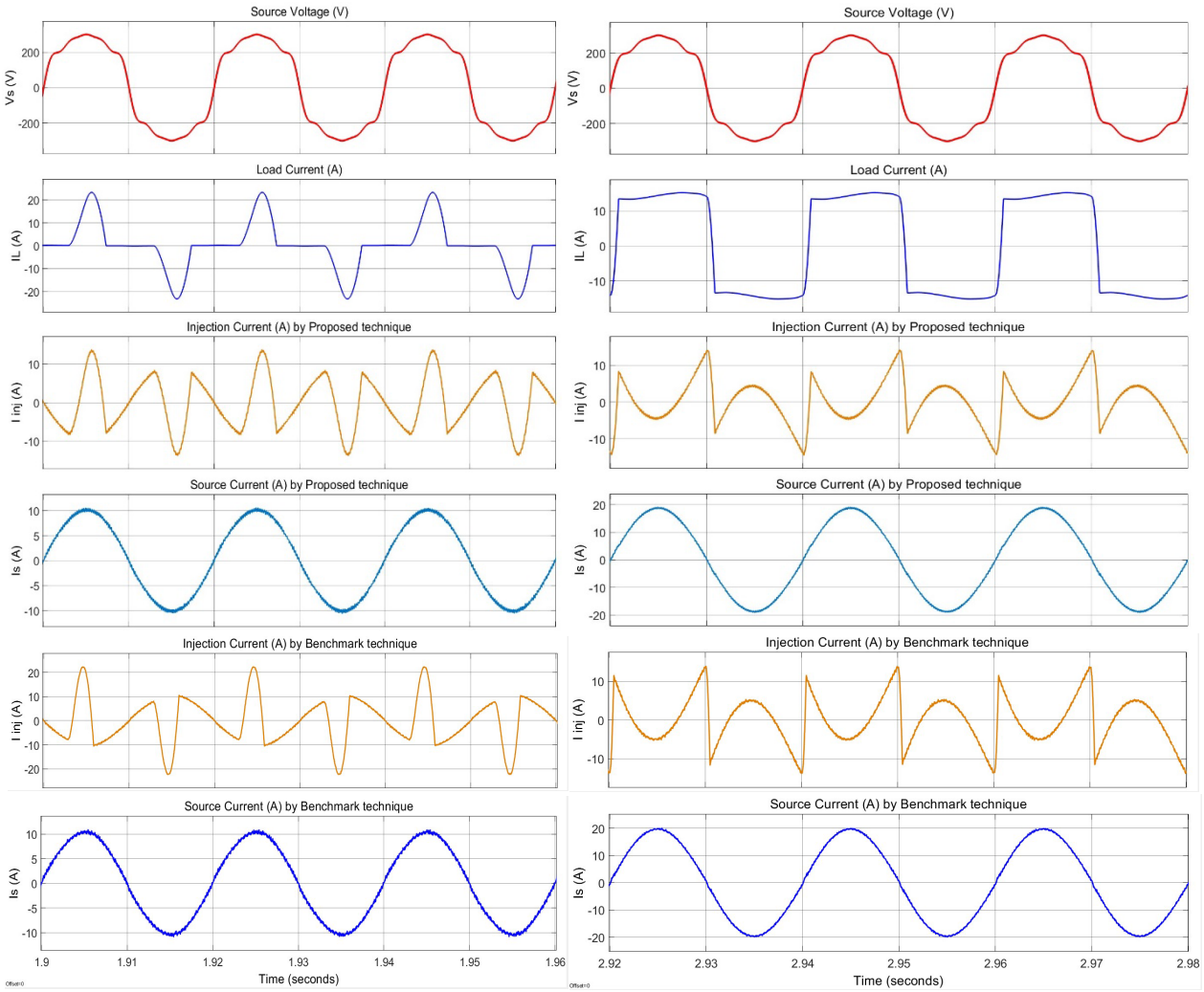


Fig. 7 *Waveforms of voltage V_s, load current I_L, injection current I_{inj} and source current I_s of proposed and benchmark techniques under (a) RC; and (b) RL load conditions*

Table 2 *THD values of source current, I_s under RC and RL load conditions*

Method	RC load (THD%)	RL load (THD%)
Without SAPF	112.22	43.31
Benchmark Technique	3.28	1.82
Proposed Technique	3.04	1.74
%Reduction	7.3%	4.4%

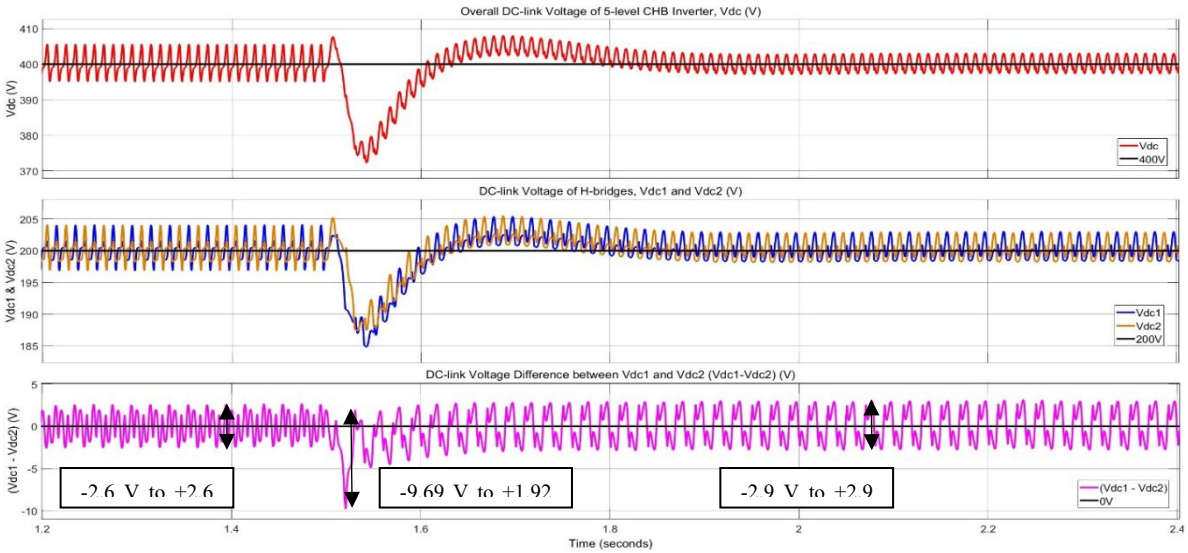
Table 3 *Phase difference of source current, I_s under RC and RL load conditions*

Method	RC load (phase difference)	RL load (phase difference)
Without SAPF	9.5	-7.9
Benchmark Technique	0.5	-0.2
Proposed Technique	0.1	0.0

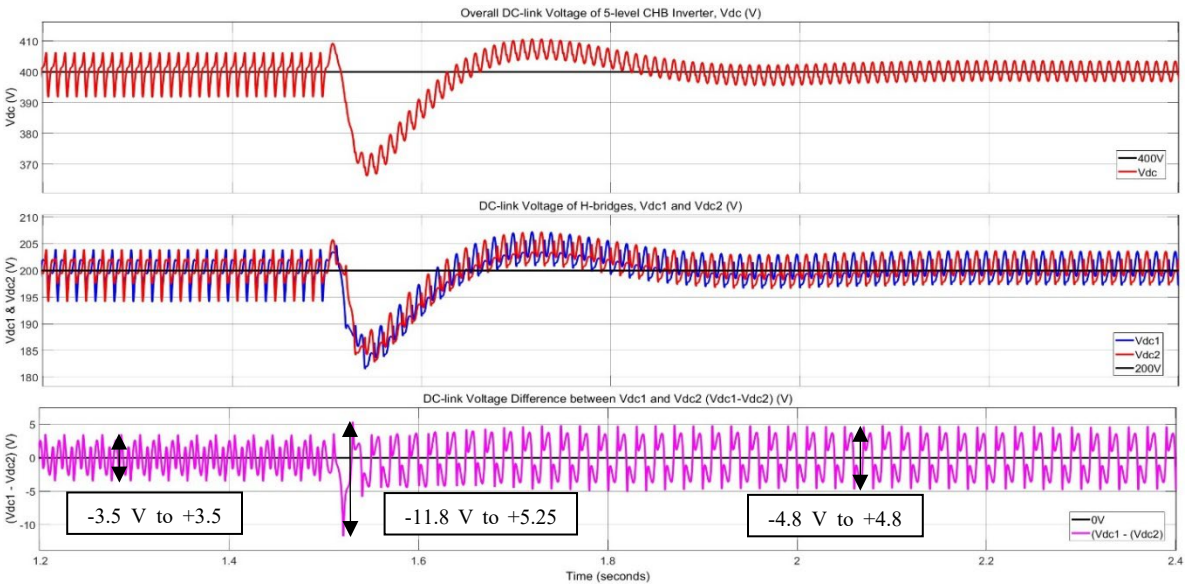
Int. Journal of Integrated Engineering Vol. 18 No. 3 (2026) p. 327-339

Table 4 *Peak-to-peak voltage ripple under RC and RL load conditions*

Load Condition	Benchmark Technique	Proposed Technique	%Reduction
Steady-state condition (peak-to-peak voltage ripple)			
RC	3.5 V to -3.5 V (total= 7 V)	2.6 V to -2.6 V (total= 5.2 V)	25.7%
RL	4.8 V to -4.8 V (total= 9.6 V)	2.9 V to -2.9 V (total= 5.8 V)	39.6%
Dynamic-state condition (peak-to-peak voltage ripple)			
RC-to-RL	5.25 V to -11.8 V (total= 17.05 V)	1.92 V to -9.69 V (total= 11.61 V)	31.9%



(a)



(b)

Fig. 8 *DC-link voltage waveforms of 5-lv CHB inverter demonstrated by (a) The proposed technique; and (b) Benchmark technique*

5. Conclusion

The results show the superior performance of the proposed voltage balancing technique compared to the benchmark technique across various operating conditions. Under steady-state conditions, the proposed technique achieved significant reductions in peak-to-peak voltage ripple, with a 25.7% reduction for RC loads and a 39.6% reduction for RL loads. Similarly, during dynamic-state conditions, the proposed technique reduced the peak-to-peak voltage ripple by 31.9% during load changes from RC to RL.

Additionally, the proposed technique consistently delivered improved harmonic mitigation and phase alignment. For THD, the proposed technique outperformed the benchmark, achieving reductions of 9% for RC loads and 7.8% for RL loads. Furthermore, the proposed technique achieved better phase alignment with negligible phase differences for both RC and RL loads.

These findings highlight the proposed technique's effectiveness in enhancing voltage balancing, mitigating harmonics, and maintaining stable operation under both steady-state and dynamic-state conditions, making it a robust and efficient solution for CHB inverter-based SAPF applications.

Acknowledgement

This research was supported by Ministry of Higher Education, Malaysia (MoHE), through Fundamental Research Grant Scheme (FRGS/1/2024/TK08/UTAR/02/4)

Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The authors confirm contribution to the paper as follows: ***Methodology, Study conception design, Literature Search and Writing – Original Draft:*** *Yong Swee Xiang;* ***Writing – Review & Editing and Supervision:*** *Yap Hoon, Hou Kit Mun, Foo Wah Low. All authors reviewed the results and approved the final version of the manuscript.*

References

[1] [1] Hoon, Y., Radzi, M. A. M., Zainuri, M. A. A. M., & Zawawi, M. A. M. (2019). Shunt active power filter: A review on phase synchronization control techniques. Electronics (Switzerland), 8(7), 791. https://doi.org/10.3390/electronics8070791

[2] Liu, Z., Peng, Z., Ou, L., Peng, X., & Wang, J. (2020). An efficiency improvement method for Si/SiC hybrid switch-based inverter. IEEE Applied Power Electronics Conference and Exposition (APEC), 1094–1097. https://doi.org/10.1109/APEC39645.2020.9124273

[3] Rana, R. A., Patel, S. A., Muthusamy, A., Lee, C. W., & Kim, H. J. (2019). Review of multilevel voltage source inverter topologies and analysis of harmonic distortions in FC-MLI. Electronics (Switzerland), 8(11), 1329. https://doi.org/10.3390/electronics8111329

[4] Singh, A., Saxena, R., & Nikum, K. (2019). Comparative analysis of two control schemes for APF with passive filter. IEEE International Conference for Convergence in Technology (I2CT), 1–6. https://doi.org/10.1109/I2CT45611.2019.9033856

[5] Rathore, S., Kirar, M. K., & Bansal, S. K. (2015). Simulation of cascaded H-bridge multilevel inverter using PD, POD, APOD techniques. Electrical & Computer Engineering: An International Journal, 4(3), 27–41. https://doi.org/10.14810/ecij.2015.4303

[6] Omer, P., Kumar, J., & Surjan, B. S. (2020). A review on reduced switch count multilevel inverter topologies. IEEE Access, 8, 22281–22302. https://doi.org/10.1109/ACCESS.2020.2969551

[7] Bharatkar, S. S., Raju, M., Bhoyar, R., Sarang, M., & Khadtare, A. (2014). Analysis of three-phase cascaded H-bridge multilevel inverter for symmetrical and asymmetrical configuration. International Conference on Automation, Control, Energy and Systems (ACES), 1–6. https://doi.org/10.1109/ACES.2014.6807993

[8] Nos, O. V., Kharitonov, S. A., Abramushkina, E. E., Brovanov, S. V., & Smirnov, P. N. (2019). Capacitor voltage balancing of cascaded H-bridge multilevel inverter. IEEE International Conference on Mechatronics (ICM), 327–331. https://doi.org/10.1109/ICMECH.2019.8722835

[9] Thajeel, E. M., Mahdi, M. M., & Abbas, E. I. (2020). Fuzzy logic controller-based shunt active power filter for current harmonic compensation. International Conference on Computer Science and Software Engineering (CSASE), 94–99. https://doi.org/10.1109/CSASE48920.2020.9142059

[10] Chokkalingam, B., Bhaskar, M. S., Padmanaban, S., Ramachandaramurthy, V. K., & Iqbal, A. (2019). Investigations of multi-carrier pulse-width modulation schemes for diode-free neutral-point-clamped multilevel inverters. Journal of Power Electronics, 19(3), 702–713. https://doi.org/10.6113/JPE.2019.19.3.702

[11] Monolithic Power Systems. (n.d.). Pulse width modulation (PWM) techniques. Retrieved January 9, 2024, from https://www.monolithicpower.com/en/power-electronics/dc-ac-converters/pulse-width-modulation-techniques

[12] Udakhe, P., Atkar, D., Chiriki, S., & Borghater, V. B. (2016). Comparison of different types of SPWM techniques for three-phase seven-level cascaded H-bridge inverter. IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES). https://doi.org/10.1109/ICPEICES.2016.7853286

[13] Hoon, Y., Radzi, M. A. M., Hassan, M. K., & Mailah, N. F. (2017). Neutral-point voltage deviation control for three-level inverter-based shunt active power filter with fuzzy-based dwell-time allocation. IET Power Electronics, 10(4), 429–441. https://doi.org/10.1049/iet-pel.2016.0240

[14] Gupta, T., & Sambariya, D. K. (2017). Optimal design of fuzzy logic controller for automatic voltage regulator. International Conference on Information, Communication, Instrumentation and Control (ICICIC). https://doi.org/10.1109/ICOMICON.2017.8279140

[15] Daher, S., Schmid, J., & Antunes, F. L. M. (2008). Multilevel inverter topologies for stand-alone PV systems. IEEE Transactions on Industrial Electronics, 55(7), 2703–2712. https://doi.org/10.1109/TIE.2008.922601

[16] Maheswari, K. T., Bharanikumar, R., Arjun, V., Amrish, R., & Bhuvanesh, M. (2021). A comprehensive review on cascaded H-bridge multilevel inverter for medium-voltage high-power applications. Materials Today: Proceedings, 45, 2666–2670. https://doi.org/10.1016/j.matpr.2020.11.519

[17] Hoon, Y., Radzi, M. A. M., Hassan, M. K., Mailah, N. F., & Wahab, N. I. A. (2016). A simplified synchronous reference frame for indirect current-controlled three-level inverter-based shunt active power filters. Journal of Power Electronics, 16(5), 1964–1980. https://doi.org/10.6113/JPE.2016.16.5.1964

[18] Kumar, U., & Kumar, S. (2020). DC-link voltage balancing with fuzzy logic controller for shunt active power filter of more-electrical aircraft. IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC), 1–6. https://doi.org/10.1109/STPEC49749.2020.9297762

[19] Oghorada, O. J. K., Zhang, L., Esan, B. A., & Dickson, E. (2019). Carrier-based sinusoidal pulse-width modulation techniques for flying-capacitor modular multilevel cascaded converter. Heliyon, 5(12), e03022. https://doi.org/10.1016/j.heliyon.2019.e03022

[20] Hoon, Y., & Ahmad, H. (2024). Voltage balancing for active power filter using dual-frequency multicarrier modulation with balanced H-bridge control. E-Prime – Advances in Electrical Engineering, Electronics and Energy, 8, 100598. https://doi.org/10.1016/j.prime.2024.100598

[21] Preeti, & Beniwal, N. S. (2012). Comparison of conventional and fuzzy P/PI/PD/PID controllers for higher-order non-linear plant with high dead time. International Journal of Scientific and Research Publications, 2(8), 1–6. http://www.ijsrp.org/research-paper-0812.php?rp=P07101