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7-level of Asymmetric MLI with Reduced Number of Switching Devices Structure for High Power-Density Achievement Using Pareto-Front Method

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Abstract

This paper presents a 7-level asymmetric multilevel inverter (AMLI) utilizing a 5-level reduced number of switching devices (RNSD) configuration, optimized for high power-density achievement. The proposed RNSD configuration is modulated with Sinusoidal Pulse Width Modulation (SPWM), achieving high output voltage quality and minimized total harmonic distortion (THD). Waveform quality is verified experimentally (THD: 4.4%) and through simulation (THD: 0.8%), adhering to IEEE Std 519-1992 requirements. A Pareto-Front analysis validates the topology's superior performance relative to the conventional 7-level cascaded H-bridge (CHB). Operating across a switching frequency range of 2 kHz to 500 kHz, the design achieves a peak power density of 4.46 kW/dm^3 at 75 kHz with a sustained efficiency of 98.52%. The AMLI with RNSD is established as a highly effective solution for advancing high-power-density converter applications.

1. Introduction

The growing demand for high-performance industrial equipment, particularly within the electric vehicle (EV) and hybrid electric vehicle (HEV) sectors, necessitates power converters capable of handling megawatt-level power and high voltage (HV) applications [1]. Multilevel inverters (MLIs) have become essential components in these systems, effectively managing battery pack voltage and operating AC traction motors [2]. Adopting HV systems reduces current demand, thereby minimizing cable size and improving overall system compactness.

For EV/HEV applications, the critical performance parameters are high efficiency and high power-density. Achieving high power-density requires a simultaneous reduction in converter volume and minimization of semiconductor power losses. While traditional cascaded H-bridge (CHBMLI) topologies are widely utilized [3], they often face limitations in reducing the total device count, which directly impacts switching losses and the resultant thermal management requirements (heatsink volume) [4]. This trade-off between power output and physical size represents a significant research gap in modern converter design.

To bridge this gap, the Asymmetric Multilevel Inverter (AMLI) topology is employed, specifically featuring a Reduced Number of Switching Devices (RNSD) structure. The AMLI with RNSD approach allows for the generation of a high-level output voltage (e.g., 7-level) with significantly fewer components than symmetric MLI structures

[5]. This reduction directly translates to minimized semiconductor losses, lower thermal stress, and consequently, a substantial reduction in heatsink volume [6][7]. The proposed RNSD circuit configuration is thus capable of achieving a demonstrably high power-density converter.

This study utilizes the 7-level AMLI with an RNSD circuit configuration, modulated using the Sinusoidal Pulse Width Modulation (SPWM) technique to ensure low Total Harmonic Distortion (THD) and high output voltage quality. The Pareto-Front technique is adopted for a performance comparison. This powerful, multi-objective optimization tool quantifies and visualizes the efficiency versus power-density trade-off, setting our results against conventional cascaded H-bridge structures across varying operating frequencies [8][9]. The paper proceeds to detail the proposed topology, the SPWM switching scheme, experimental validation, and the final Pareto-Front analysis

2. High Power-Density Achievement Consideration

The industry began to demand high-performance equipment which now has reached megawatts level and will grow further

2.1 Reduced Number of Switching Devices (RNSD) Circuit Structure

Traditional Cascaded H-Bridge Multilevel Inverters (CHBMLI) are effective for high-voltage applications but suffer from a rapidly increasing component count as the output voltage level is increased [10]. This higher number of switching devices leads to greater semiconductor losses (conduction and switching losses), which directly impacts overall system efficiency and necessitates larger heatsinks, thereby reducing power-density.

To overcome this limitation, we propose a novel 7-level Asymmetric Multilevel Inverter (AMLI) realized by a 5-level RNSD structure. The proposed structure is conceptually divided into two functional stages: Level Generation Stage (S1, S2): This front-end stage, comprising switches S1 and S2 and their associated asymmetric DC sources, is responsible for generating the positive voltage steps. Polarity Switching Stage (SA through SD): This section, configured as a standard H-bridge, performs the essential polarity reversal of the output voltage. By leveraging the AMLI binary DC source ratio and this two-stage design, the proposed RNSD topology in Fig.1 achieves a 7-level output using only six active switching devices. This offers a significant advantage in component count compared to the conventional 7-level CHBMLI structure in Fig.2, which requires twelve switching devices for the same output quality. This reduction directly minimizes system losses and enables the high power-density focus of this work.

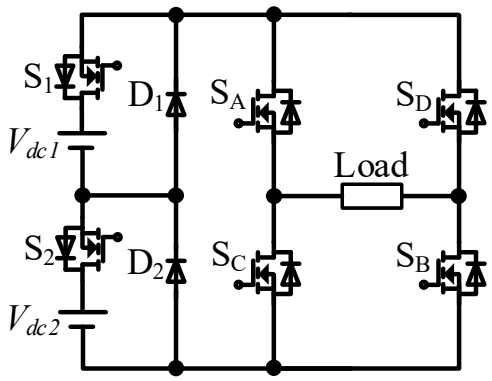

Fig. 1 *Proposed 7-level RNSD configuration*

Int. Journal of Integrated Engineering Vol. 17 No. 9 (2025) p. 1-11

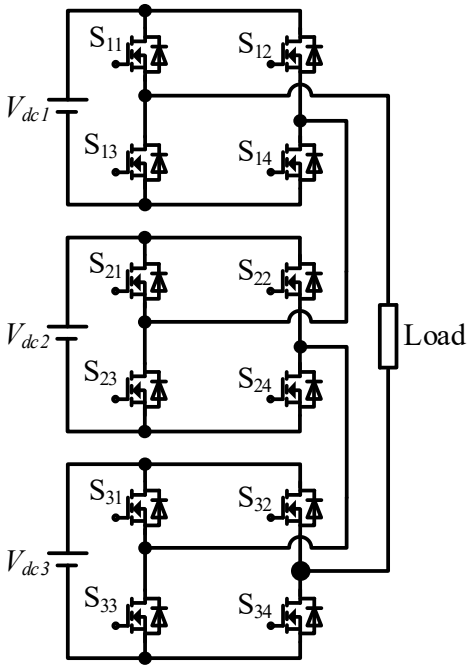

Fig. 2 *Conventional 7-level CHBMLI configuration*

2.2 Volume Reduction of Passive Components

The efficiency and power density of the proposed AMLI with RNSD configuration are heavily dependent on minimizing the volume of passive components (i.e., filters). To achieve high power density, the output voltage THD must be inherently low, minimizing the size requirements of the necessary LC passive filter [11].

There are three primary methods for THD reduction in multilevel inverters. The first involves increasing the output voltage levels (e.g., moving from 5-level to 7-level), which produces a staircase waveform closer to a pure sine wave, intrinsically reducing THD [12]. However, this approach traditionally requires a proportional increase in the number of switching devices, leading to greater complexity, higher losses, and increased volume—the core challenge the RNSD topology is designed to solve. The second category includes optimal switching angle methods [13], such as Selective Harmonic Elimination (SHE) or using Artificial Intelligence (AI) to manage switching angles. While effective for specific harmonic removal, these methods often involve intricate control schemes and mathematical limitations on which harmonic orders can be eliminated. The third and often most straightforward approach is the selection of the modulation strategy, employing advanced Pulse Width Modulation (PWM) techniques like MPWM or SPWM for effective THD management [14].

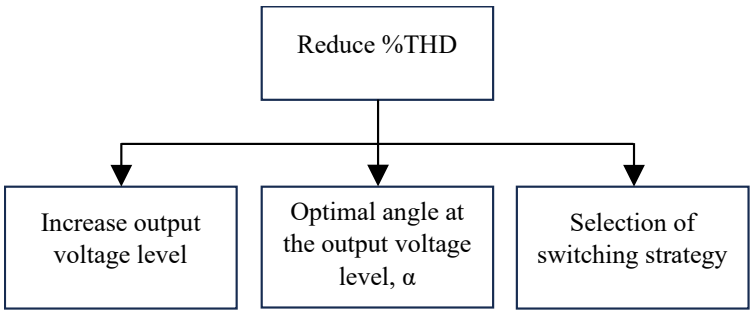

Fig. 3 *Reduction of THD*

For the proposed 7-level AMLI with RNSD configuration, the Sinusoidal Pulse Width Modulation (SPWM) technique is adopted. SPWM is selected because its reference signal is a sine wave, resulting in an output waveform that inherently possesses a lower THD compared to other modulation methods. However, it must be acknowledged that SPWM typically operates at a high switching frequency, which usually results in increased switching losses. Our proposed RNSD topology, by virtue of its dramatically reduced switch count (six devices for 7-level output), effectively mitigates these switching losses, allowing us to leverage the superior THD performance of SPWM without compromising overall system efficiency.

2.3 Asymmetric Topology

Each DC source voltage in an RNSD circuit configuration may or may not be equal. It is referred to be SMLI if all DC source voltages are the same. It's AMLI, though, if every DC supply voltage varies. The SMLI operation operates on the same principle as CHBMLI, with the output voltage level limited to a specific number of levels and dependent on the number of switching devices utilized. The most common DC sources voltage in AMLI are those with binary and ternary ratios [15]. The voltage levels in binary progression will be (2^{N+1-1}) and the DC source voltages will have a ratio of 1: 2: 4: 8...: 2^N. In the meantime, the voltage levels will be (3N) and the ternary progression displays the amplitude of DC source voltages with a ratio of 1: 3: 9: 27...: 3^N [16]. N is the number of voltages from DC sources.

Without altering the conventional or SMLI [17] structure, AMLI has the advantage of being able to generate higher output voltage levels. However, it uses a different DC source voltage; the AMLI topology has different DC source voltages, such as Vdc1 = Vdc, Vdc2 = 2Vdc, and Vdc3 = 4Vdc, compared to the DC source voltages of SMLI, which are Vdc1 = Vdc2 = Vdc3. The complicated AMLI topology switching method allows for level upgrades of up to two tiers. The suggested RNSD circuit structure for the 7-level AMLI is displayed in Fig. 2. There is a clear disparity in the quantity of switching devices between the two structures. For a better understanding, see Fig. 4's concept graph of the SMLI and AMLI topologies that have been applied to the RNSD circuit topology. Essentially, even while employing the same circuit, AMLI's voltage THD and number of switching devices are superior to those of SMLI and traditional MLI.

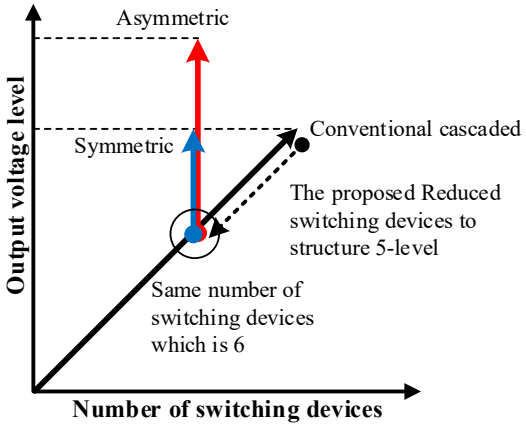

Fig. 4 *Concept of the proposed RNSD circuit structure with symmetric and asymmetric topologies*

3. Pareto-Front Method

An assessment technique called Pareto-Front can be used to identify the ideal combination of power density and efficiency. Power losses and converter volume are the primary Pareto-Front characteristics, as they are necessary for estimating efficiency and power density [18]. Volume in dm^3 is the primary factor in calculating power density, which is expressed in kW/dm3. As a result, the Pareto-Front principle assesses two factors to determine which converter structure achieves the highest efficiency and power density [19]. The graph of power density against efficiency's optimal point for each construction is depicted by the curves.

3.1 Power Losses and Efficiency Principles

The overall performance of the proposed converter is assessed through a comprehensive power loss analysis, as system efficiency is inversely proportional to total power losses P_{loss} [20]. Theoretically, minimizing P_{loss} directly enhances converter efficiency. In essence, power losses is defined as the sum of losses from all primary components in the system:

$$P_{loss} = P_{SM} + P_{Cap} + P_L \tag{1}$$

where P_L is the inductor loss, P_{SM} is the semiconductor loss, and P_{Cap} is the capacitor loss. Semiconductor losses are expressed as follows and are the total of two losses:

$$P_{SM} = P_{SW} + P_{cond} \tag{2}$$

where P_{cond} is the conduction loss and P_{SW} is the switching loss. The two main categories of losses in switching devices are switching loss and conduction loss, calculated using Equation (3) and Equation (4), respectively.

Equation (3) involves the device's voltage stress, which is critical for determining the device rating and selection. The switching loss specifically occurs during the rise and fall times (t_r+ t_f) of the switching cycle. Crucially, the overall P_{SW} for the converter is the cumulative sum across all switches. Since the SPWM strategy involves a higher operating frequency compared to, for instance, a MPWM strategy, it inherently results in greater P_{SW} due to faster "ON" and "OFF" operations [21]. However, the proposed RNSD topology minimizes the total P_{SW} by drastically reducing the number of devices required. The total switching loss across the converter is the sum of P_{SW} for all six active switches. Conduction Loss is further divided into MOSFET and diode losses. The MOSFET conduction loss is calculated as Equation (4).

$$P_{sw} = \frac{I_{DS} \times V_{DS} \times (t_r + t_f) \times f_{sw}}{6} \tag{3}$$

$$P_{cond} = {I_{DS}}^2 \times R_{DS(ON)} \times D \tag{4}$$

I_{DS} is the diode-source current and V_{DS} is the drain-source voltage. $R_{DS(ON)}$, on the other hand, is the MOSFET's on-resistance depending on the device rating. f_{sw} is the switching frequency and D is the duty cycle determined by the multilevel inverter's switching pattern. It is important to note that P_{cond} is independent of the switching frequency. The proposed RNSD structure includes two diodes, necessitating the calculation of diode conduction loss, $P_{condDiode}$:

$$P_{condDiode} = V_{Diode.on} \times I_{in} \times (1 - D) \tag{5}$$

where I_{in} is the current flowing through the diode, (1−D) is dependent on the circuit configuration's operating mode, and $V_{Diode.on}$ is based on the component rating, also referred to as forward voltage. The losses for the semiconductor losses are found by adding the values from Equations (3), (4), and (5).

The LC passive filter is one of the passive components used in this study's loss analysis based on a filtering circuit. Consequently, the following is the computation for inductor loss, P_L and capacitor loss, P_{Cap}:

$$P_{Cap} = {I_{rms}}^2 \times R_{ESR} \tag{6}$$

$$P_L = {I_{rms}}^2 \times R_L \tag{7}$$

where R_{ESR} is the equivalent series resistance based on the equivalent series resistance of the capacitor, and I_{rms} is the root mean square of the output current. While R_L is the inductor's winding wire resistance. The formula for calculating efficiency, η looks like this:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \tag{8}$$

$$P_{out} = P_{in} - P_{loss} \tag{9}$$

where P_{in} represents the input power and P_{out} the output power. Efficiency is a crucial metric for assessing the multilevel inverter's performance. Equation (8) displays the efficiency in percentage.

3.2 Principles of volume and power density

Typically, the converter's overall volume is the total of multiple volumes. Volume is a crucial factor that must be taken into account in order to calculate the converter's potential for power density [22]. The power density's brain is called volume [18]. Consequently, the following equation is used to determine the converter's total volume, Vol:

$$Vol = Vol_H + Vol_{Cap} + Vol_L \tag{10}$$

where Vol_L is the inductor's volume, Vol_{Cap} is the capacitor's volume, and Vol_H is the heatsink's volume. Equation (10), which can be applied to obtain the converter's total volume. The following formula can be used to determine the heatsink's volume:

$$Vol_H = \frac{P_{SW} + P_{cond}}{(T_j - T_a)CSPI} \tag{11}$$

where T_a is the switching devices' ambient temperature, P_{SW} is their switching loss, P_{cond} is their conduction loss, T_j is their junction temperature, and $CSPI$ is their cooling system performance index. The following formula is used to get the capacitor's volume:

$$Vol_{Cap} = length \times width \times height \tag{12}$$

where the dimensions of the capacitor are its length, breadth, and height, which are determined by its shape. The next formula is used to determine the inductor's volume. The inductor's volume is calculated based on its energy storage capability, core configuration, and current density:

$$Vol_L = K_v(\frac{2W}{K_u B_m J_w})^{\frac{3}{4}} \tag{13}$$

where W is the maximum energy of the inductor, J_w is the current density of the winding wire, B_m is the flux density, K_v and K_u are the constant value established by the core's configuration. The maximum energy, W of the inductor is defined by:

$$W = \frac{LI^2}{2} \tag{14}$$

where I represent the inductor's current flow and L its inductance. With the total volume established, the final performance of power density, ρ which is the primary contribution of this work, is calculated as the ratio of output power P_{out} (kW) to the total converter volume, Vol_{total} (dm^3):

$$\rho = \frac{P_{out}}{Vol_{total}} \tag{15}$$

4. Analyses and Results

Sub-topics 4.2 and 4.3 describe volume analyses and losses. The study's findings are broken down into two sections. The first part discusses the suggested RNSD structure and shows that it can provide the intended output voltage by simultaneously observing the voltage THD before and after the filter. The results of a comparison between the suggested RNSD and traditional cascaded circuit architectures are displayed in the second section, which describes how high power-density was achieved utilizing the Pareto-front technique.

4.1 RNSD Structure

Table 1 presents the total harmonic distortion (THD) results for the pre-filter output voltage, comparing the proposed RNSD structure operating under the SPWM strategy in both SMLI (5 levels) and AMLI (binary, 7 levels) modes. The data confirms the fundamental advantage of the AMLI topology by utilizing an asymmetric DC source ratio, it inherently generates a higher output voltage level (7 levels) with the same number of active switches as the 5-level SMLI. This greater number of voltage steps creates a staircase waveform that more closely approximates a pure sine wave, resulting in a significant THD reduction from 26.92% (SMLI) to 18.33% (AMLI) in simulation and 26.40% to 17.75% in experimental results, successfully validating the low-level harmonic suppression theory.

Table 1 *Voltage THD based on SMLI and AMLI topologies*

Topology	Level of Output Voltage	THD voltage (%) SPWM switching strategy	
		Simulation	Experiment
SMLI	5	26.92	26.40
AMLI (binary)	7	18.33	17.75

The voltage THD results for the proposed 7-level asymmetric converter (RNSD topology) are summarized in Tables 1 and 2. After filter implementation, the THD was significantly reduced from 18.33% (simulation) and 17.75% (experiment) as shown in Table 1 to 0.8% (simulation) and 4.4% (experiment) as shown in Table 2, respectively. Based on the resonant frequency theory, the inductance and capacitance estimations are used in the suggested 7-level asymmetry employing the SPWM switching technique. The highest output voltage of 166 V, as indicated by the experimental results in Fig. 5(a), is consistent with the findings of the simulation. The maximum output power of 300 W is indicated by the maximum output current of 1.8 A. It is verified by looking at the experiment results of the suggested 7-level AMLI that the suggested circuit topology functions properly, even with fewer switching devices that adhere to the asymmetry principle. Additionally, it demonstrates that the chosen switching strategy is able to run the switching devices in a way that corresponds with the circuit structure's operating mode.

Int. Journal of Integrated Engineering Vol. 17 No. 9 (2025) p. 1-11

Table 2 *Voltage THD after filter between simulation and experimental results*

Level	%THD voltage at V_{out} (Simulation)	%THD voltage at V_{out} (Experiment)	Filter specifications	
			L (mH)	C (μF)
7	0.8	4.4	30	4.5

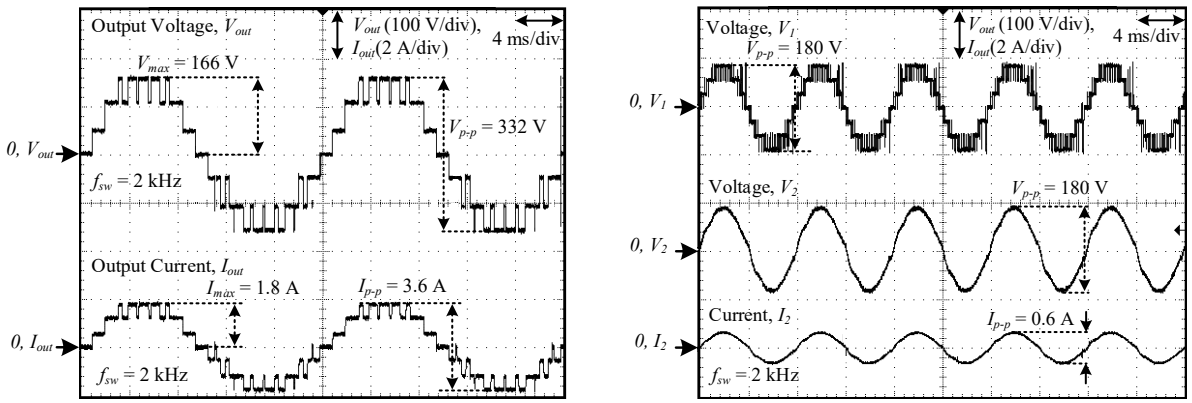

Fig. 5 *Results of experiments with the suggested 7-level AMLI of RNSD circuit topologies employing an SPWM switching technique (a) The output voltage level, (b) The output voltage level with filter*

Because switching is not implemented with the same accuracy as the experiment's simulation, Table 2's voltage THD differs. As a result, the multilevel inverter's output voltage before filter is different from what was anticipated, as shown in Fig. 5(b), which displays the experiment's findings. The observable difference between the simulated THD (0.8%) and the experimental THD (4.4%) is attributed to the presence of real-world non-idealities that are excluded from the ideal simulation environment. These factors include the dead-time effects which the practical implementation of the SPWM control introduces necessary dead-time between switching transitions, which distorts the output voltage near the zero-crossing points. It also can due to the component tolerances where the variations in the passive component values (inductance and capacitance) from their nominal ratings and another factor is measurement noise which the high-frequency noise introduced by current and voltage sensors and the digital signal processing (dSPACE) controller used for generating the switching signals. Despite this necessary deviation, the experimental result remains well below the 5% limit, confirming the proposed structure's robust performance under practical conditions. To ensure reproducibility, the experimental validation was conducted using a DC power supply, switching devices (rated 1.5 to 2 times above the voltage limits), a resistance load, and a power analyzer for accurate THD measurement. The maximum output voltage achieved was 166 V at 300 W output power, as confirmed by Figure 5(a) and (b).

4.2 Power Losses Analyses and Efficiency

A critical analysis of the power loss principles was performed for both the proposed 7-level AMLI with RNSD structure and the conventional 7-level CHBMLI to clearly quantify the advantage of the reduced switch count. All calculations were conducted at a high switching frequency of 500 kHz to emphasize the impact on switching losses. As demonstrated in Figure 6, the proposed RNSD structure successfully reduced the total power losses from the CHBMLI's 14.83 W down to 6.66 W. This massive reduction is primarily attributed to the RNSD topology requiring only six switching devices compared to the conventional structure's twelve, directly mitigating the semiconductor losses (conduction and switching losses). Specifically, the reduced component count significantly lowered the contribution of both conduction and switching losses to the total loss budget. This substantial decrease in power losses directly translates to higher efficiency. Based on a maximum output power of 300 W and the calculated 6.66 W in total losses, the proposed 7-level AMLI (RNSD) achieves a high overall efficiency of 98.52%. This figure clearly demonstrates the superior performance of the RNSD structure over the conventional cascaded configuration.

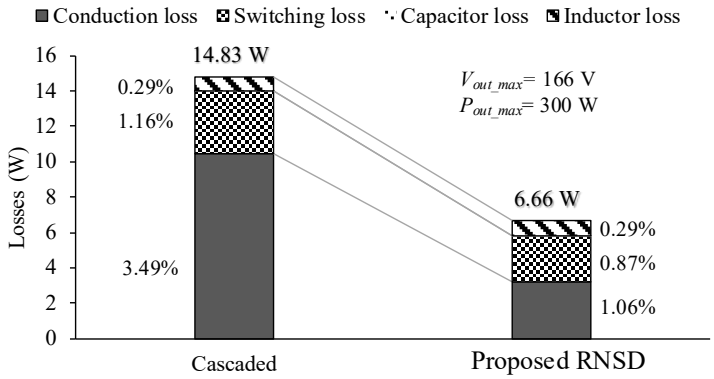

Fig. 6 *Loss calculations using two different kinds of structures*

4.3 Volume Analyses and Power Density

The analysis confirms that the total converter volume (Vol_{total}) is the critical factor for maximizing power density. Figure 7 illustrates the volume breakdown, where the inductor (Vol_L) and capacitor (Vol_{Cap}) volumes remain constant (at 0.0597 dm^3) because their design is fixed by the resonant frequency and filter specifications. As demonstrated by the significant reduction in semiconductor losses (from14.83 W to 6.66 W), the thermal requirements are drastically lessened. This enables a large reduction in Vol_H, which is directly determined by the total semiconductor losses. Figure 7 clearly illustrates this advantage: the heatsink volume is reduced by a remarkable 58.5% for the proposed RNSD structure compared to the conventional cascaded configuration. This substantial decrease in the heatsink component leads to a reduction in the total converter volume from 0.0877 dm^3 (Cascaded) to 0.0714 dm^3 (Proposed RNSD). This minimized volume, when combined with the maximized output power (300 W), results in the final of Power Density. By optimizing both efficiency (low loss) and volume, the proposed RNSD circuit configuration successfully achieves a superior power density performance, which serves as the final justification for the proposed structure.

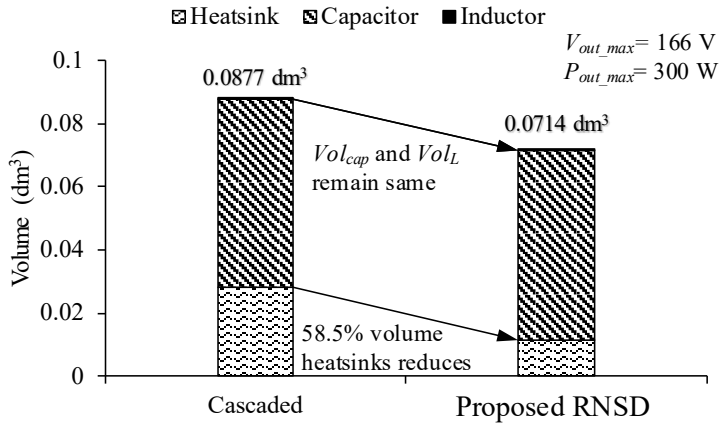

Fig. 7 *Total volumes using the suggested RNSD structure and cascaded*

4.4 Pareto-Front Curves

The final performance of the proposed structure is validated using the Pareto-Front technique, a powerful multi-objective optimization tool used to quantify the critical trade-off between Efficiency and power density. Figure 8 depicts the Pareto-Front curves for the conventional 7-level CHBMLI structure and the proposed 7-level AMLI with the RNSD configuration. The Pareto-Front curve for the proposed RNSD structure is distinctly superior, positioned much higher and further to the right on the plot, confirming that it achieves a higher power density at any given efficiency point compared to the CHBMLI. The optimal operating point for the RNSD is clearly identified at a switching frequency of 75 kHz, where it achieves a maximum power density of approximately 4.4 kW/dm^3 while maintaining a high efficiency of 98.52%. This superior positioning is a direct result of the design choices: the RNSD structure's reduced switch count leads to significantly lower losses (maximizing η), which in turn drastically reduces the heatsink volume (maximizing power density). The analysis confirms the successful mitigation of the efficiency-power-density trade-off. Consequently, the proposed RNSD configuration is capable of

delivering a smaller, more compact, and higher power-density converter, making it highly attractive for manufacturers interested in size-constrained power applications, particularly in sectors like transportation. The 7-level output was strategically chosen for this comprehensive evaluation because it provides the clearest point of differentiation; at this voltage level, the benefits of the RNSD structure in terms of loss reduction and volume minimization are most easily and significantly demonstrated.

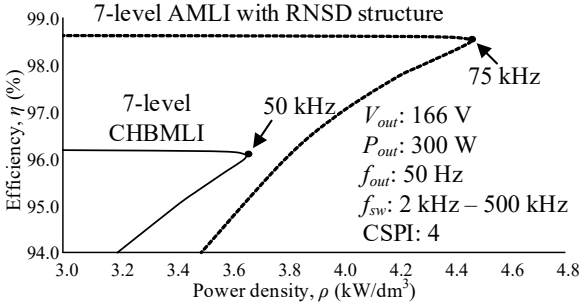

Fig. 8 *Pareto-Front of the proposed 7-level RNSD and the 7-level cascaded H-bridge structure*

5. Conclusion

The proposed Reduced Number of Switching Devices (RNSD) structure successfully resolves the fundamental trade-off between efficiency and power density in multilevel inverters. The key to this achievement lies in the 7-level asymmetric topology, which utilizes only six active switches—a significant reduction compared to conventional cascaded structures. This minimization of components directly results in a substantial reduction of total semiconductor losses (down to 6.66 W), which in turn permitted a 58.5% reduction in the thermally critical heatsink volume. The final validated performance metrics confirm the structure's superiority where the RNSD achieved a peak power density of 4.46 kW/dm^3 at the optimal 75 kHz operating point, while simultaneously maintaining a high efficiency of 98.52%. This outcome demonstrates that the proposed structure successfully pushes the Pareto-Front boundary outward, securing an optimal design that is highly compact and thermally efficient. This research provides a validated topology for realizing high power-density converters, which is crucial for modern industrial applications, particularly in the transportation sector (e.g., electric vehicle powertrains) where size and weight are paramount constraints. Future work will focus on two key directions which are implementing advanced Model Predictive Control (MPC) strategies to further refine harmonic performance without increasing switching losses, and investigating the integration of wide-bandgap (SiC/GaN) devices to potentially push the maximum power density point beyond 5 kW/dm^3.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

*In this study **conception and design** was developed by Mohd Hafizie Yatim; **data collection** by Mohd Hafizie Yatim; **analysis and interpretation of results** by Mohd Hafizie Yatim, Asmarashid Ponniran, Mohd Amirul Naim Kasiran; **draft manuscript preparation** by Mohd Hafizie Yatim, Asmarashid Ponniran, Mohamad Kamil Romai Noor, Rini Nur Hasanah, Waru Djuriatno. All authors reviewed the results and approved the final version of the manuscript.*

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