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Design of Miniaturized On-chip Monopole Planar Antenna with Loaded Interdigital Capacitor for 5.8 GHz Devices

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Abstract

Miniaturization of the on-chip antenna (OCA) in the lower frequency band is limited by the requirement for a compact chip size imposed by the larger electrical wavelength. At the same time, shrinking the antenna size reduces radiation characteristics and incurs significant losses due to lossy silicon substrate. This paper introduces a design for a miniaturized monopole planar on-chip antenna utilizing an interdigital capacitor (IDC) as an approach. The design incorporates a partially reflective surface (PRS), characterized by a high impedance surface, into the stacked structure to enhance antenna performance at a resonant frequency of 5.8 GHz. The stacked-up structure comprises a six-layer metal-insulator-semiconductor (MIS) integrated onto a monolithic silicon substrate as the host material. A model prototype was fabricated using a sputtering process, resulting in a size reduction of 45.62 % compared to conventional designs, well-suitaed for the applications of RFIC, Wi-Fi, WiMAx, RFIC, and wireless transceivers at 802.11a. The fabricated antenna is validated and realizes an improved gain of 28.63 % and a radiation efficiency of 25.26 %, with an impedance bandwidth of 0.73 GHz at a return loss of about 20 dB.

1. Introduction

In recent years, there has been an increase in the development of modern, energy-efficient, low-profile, and high-speed for upcoming mobile and associated wireless gadgets in mid and low-frequency domains. These devices demand compact footprint antennas for optimal performance. An on-chip antenna (OCA) technology is acknowledged as a promising and advanced integrated antenna solution for compact wireless systems. It represents a significant chip-based antenna innovation that facilitates silicon integration with RF front-end components on a unified substrate [1], [2]. It is a potential antenna that is promising for extensive application. These applications include wireless transceivers, wireless fidelity, and Internet-of-Things based on users' demand [3]. It offers logical integration into small-size front-end transceivers, mainly in the application of mid-frequency, mm-wave, and beyond, with the capacity to facilitate high-speed communication [4], [5]; OCA can be integrated into the host devices using one of the two significant modules: a single-chip module (SCM) or a multi-chip module (MCM) module [6]. The innovation of on-chip antennas operating at frequencies below 10 GHz is garnering significant attention due to the growing number of applications. IoT devices, wireless transceivers, and wireless power transfers are at the forefront of this trend. Many of these devices are designed to function at low and mid-

range frequencies. For example, IoT is anticipated to be the next significant advancement in wireless technology, promoting extensive societal connectivity, according to Transform Insights TAM. There were approximately 7.6 billion active IoT devices in late 2019, projected to exceed 24 billion by 2030[7]. Thus, with this wave, a substantial amount of power is required.

Thus, to achieve perfect integration, it needs to be miniaturized with enhanced performance [8]. Despite its promising applications, real-time implementation encounters notable hurdles stemming from the limited amplification and ineffective radiation caused by the low resistivity and high-dielectric properties of the silicon (Si) substrate [9]. The low-resistivity property can lead to the confinement of incidence waves within itself, resulting in significant losses. This phenomenon severely impacts the overall performance [2], [10]. The primary concern lies in the challenge of miniaturization below 10 GHz, which is the larger electrical wavelength [11] and unsuitable for integration on footprint chip size [12]. Therefore, a miniaturized, enhanced performance design is to realize a reasonable size reduction by keeping the desired frequency constant [13], [14].

Previously, various methods for miniaturization have been suggested and tested, tailored to specific frequencies and intended uses. Among these, LC-loading [15], mender line, slow wave, metamaterial loading [16], near-field resonant parasitic (NFRP), fractal geometries, and slot-loading [17], [5] have emerged as the most widely utilized techniques. Others are partial shield layers (PSL) [18] and the loop loading method [19]. Several procedures can be employed in the quest for miniaturization, including modifying the radiator's physical geometry, controlling electromagnetic properties, altering electrical wavelengths, or integrating novel materials [20].

In [21], an LC-loading, meander line, and interdigital capacitor (IDC) were incorporated into a monopole planar antenna. The fabricated design achieved a reduced antenna length of 0.077λo, much smaller than a quarter-wavelength. [22], proposed a slow-wave technique where varactors control the operating frequency by shortening vias to the ground conductor on non-radiating edges. The method shows good matching and radiation performance. This study proposed a compact monopole-planar on-chip with loaded IDC. The model has incorporated a partially reflective periodic structure as a performance improvement method, like frequency selective surface (FSS) [23]. The combined structure offered a miniaturized and enhanced performance on-chip antenna resonating at 5.8 GHz, considering IDC as a miniaturization technique, resulting in a significant geometrical reduction of 45.61 % compared to the initial quarter wavelength model. However, it controls the total reactance of the periodic element and regulates radiation resistance through the enhanced distribution of the E-field across spatial wavelengths [24]. It has been proposed for many other resonance and charge control functions—for example, charge-flow transistor design [25].

Moreover, evading the degraded performance due to miniaturization, specifically, the radiation resistance and the gain, a PRS is embedded within the SiO_2 layer to obstruct the back radiated signal emanating from the top OCA into the lossy Si-substrate. It is an arrangement of a regular metal film of thickness 1µm with equal separation. Achieving complete restriction of EM waves is ideally impossible due to the limitation imposed by a complementary metal-oxide semiconductor (CMOS metallization rule, as the entire metal density is restricted to 20-80% [3]. Moreover, the significance of this work includes the following.

- The antenna's resonance can be adjusted to a desired frequency below 5.8 GHz without altering its dimensions. This tuning is accomplished by modifying the width of the fingers and the spacing between them, as shown in Fig. 3.
- The proposed model provides improved gain and radiation characteristics compared to similar work at 5.8 GHz cited in this work.
- Using IDC reduced the antenna's size and significantly improved the radiation pattern by generating a fringing E-field across the series, leading to better radiation performance.
- The PRS structure not only enhances the gain significantly but also reduces the number of metallization layers, utilizing only three metal layers

This article is organized into the following sections: Section 2 discusses the design and configuration of the proposed antenna with an analysis of IDC and PRS structures. Section 3 discusses the simulation results, prototype fabrication, and validations. Hence, the conclusion in Section 4 summarizes all the results.

2. Proposed Antenna Design

2.1 Antenna Model and Configuration

The proposed OCA adheres to the design principles of a typical silicon chip, with the structure being composed of stacked layers of metal, silicon, and its oxide [26]. A monopole planar antenna loaded with an IDC is integrated into the top metal layer as a radiating element. A PRS is embedded within the SiO_2 layers and functions as a reflective surface, redirecting incident waves away from the absorbent silicon substrate. Thus, the periodic arrangement PRS is electrically complemented by a ground reflector at the bottom of the Si substrate. The antenna was primarily constructed using six stacked layers comprising three layers of metal film (M1, M2, and M3), each with a thickness of 1 µm. These metal layers were positioned on a 500 µm silicon (Si) wafer, stacked within 4 µm

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thick SiO_2 layers. The topmost layer, M1, served as the antenna and was designed as a miniaturized monopole-inspired IDC. Embedded within the SiO_2 layers, the M2 component was partially reflective conductor. An M2 is a depleted ground conductor deposited beneath the silicon wafer, also structured as a PRS. The silicon substrate used as the host material had a dielectric constant (Ɛr) of 11.9 [7] and a resistivity ranging from 1-20Ω-cm [27],[28]. The proposed model's top and side views and the stack-up geometry are depicted in Fig.1(a), (b), and Fig. 2, respectively. A coplanar waveguide (CPW) feeding method was employed to connect to the coaxial port. The optimized parameters are outlined in Table 1.

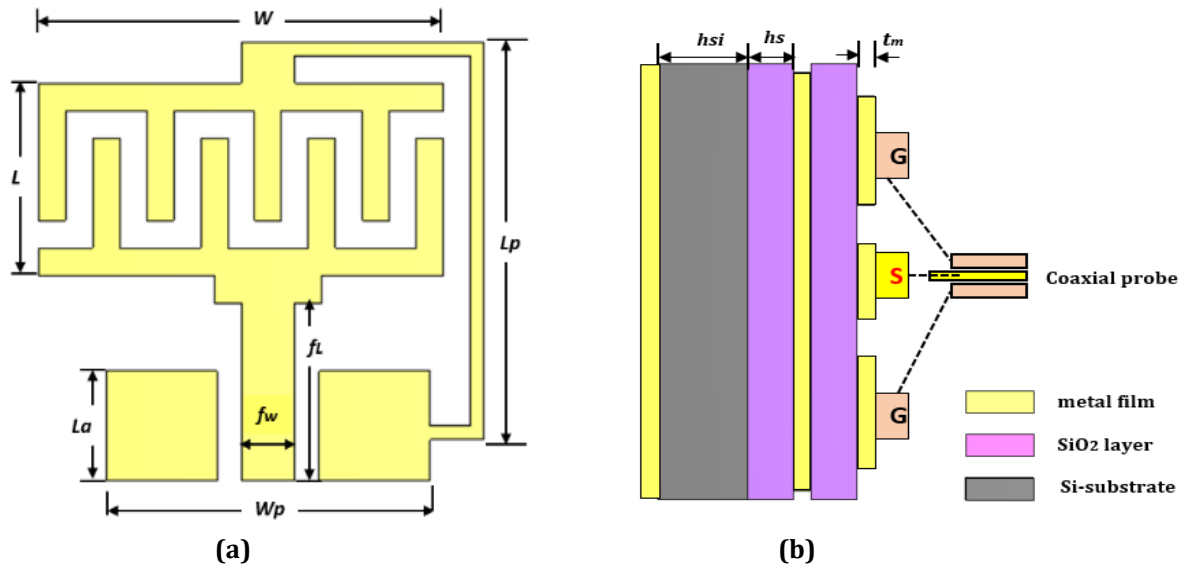


Fig. 1 *Geometry of the proposed OCA (a) Top view; (b) Side view*

Table 1 *Optimized antenna parameters*

Parameter	Value (mm)	Parameter	Value (mm)
L	3.35	*fw*	1.0
tm	0.0017	*Lp*	7.25
hs	0.02	*La*	2
W	7.15	f_L	3.25
hsi	0.525	*Wp*	5.9

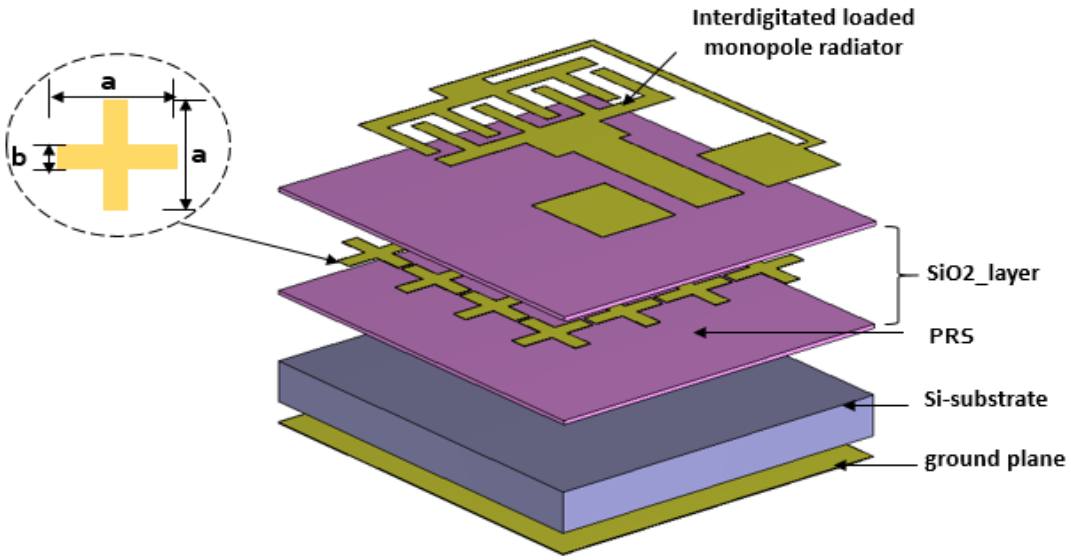
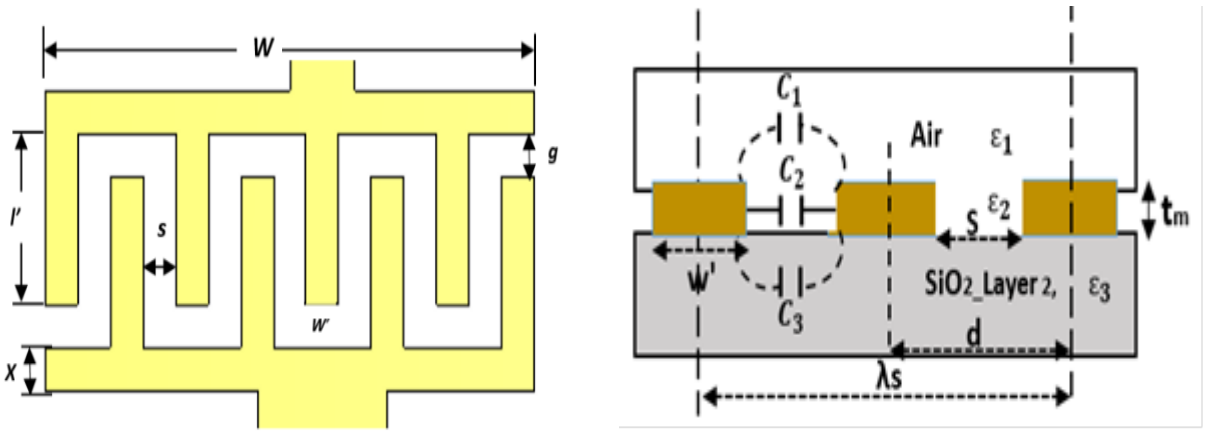


Fig. 2 *Isometric view of proposed OCA*

2.2 Design of Interdigital Capacitor

An interdigital capacitor (IDC) is a periodic arrangement characterized by a multi-finger geometry, depicted in Fig. 3(a). It exhibits a component of a lumped element and features a unit capacitance between the fingers separated by a distance 's,' with a thickness 'tm' and width 'w.' The unit capacitance, influenced by electric field fringes, correlates with the spatial wavelength λs, as illustrated in Fig. 3(b). The λs value notably influences the strength of the field between the electrodes [25]. The spacing between the electrodes is quite long and folded within a small area. IDCs are quasi-lumped elements [29] that manipulate frequency turning and impedance. A geometric arrangement of IDC minimizes parasitic capacitors of a substrate on which the component is integrated [24]. Thus, an optimized geometric parameter of the IDC is shown in Table 2. The significant advantage of IDC is that it is easy to increase the capacitance of elements by increasing the fingers and using thin, high dielectric material beneath the conducting film [30]. For example, some studies use series-coupled capacitors with similar features to IDC to control impedance bandwidth [31],

In this work, the quasi-lumped component of IDC, including the total capacitance across the fingers C_T and total inductance of parallel length L, is expressed in equations (6) and (11). The details of this analysis are given in sub-section 5, on a model equation.



(a) **(b)**

Fig. 3 *Geometrical structure of interdigitated capacitor (a) Top view; (b) Isometric view*

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Table 2 *Optimized IDC parameters*

Parameter	Value(mm)
s	0.50
g	0.50
x	0.52
W	7.15
l	7.26
w'	0.51
l'	2.0
N	8

2.3 Partial Reflective Surface

A PRS consists of a structured arrangement of metallic film positioned between the upper radiating component and a silicon substrate. Its operational characteristics resemble those of an artificial magnetic conductor (AMC). The PRS hinders the propagation of electromagnetic energy from the top radiating conductor into the silicon substrate, which is prone to losses. This arrangement can be customized to regulate the intensity of the reflected wave and manage the antenna resonance [32]. For instance, in the CMOS design procedure, an integrated periodic arrangement of a reflective metal strip within the SiO_2 layer partially obstructed an electromagnetic wave emitted by the radiator from penetrating into the lossy Si-substrate [33]; as a result, losses are minimized, and there is an improvement in both gain and radiation efficiency. This design configures a periodic array of 4x4 unit cells of 1 µm metal thickness, a square length of 4 mm2, and a width of 2 mm as an aperture. The structure was embedded within the SiO_2 as the third layer from the top, as shown in Fig. 2.

2.4 Analytical Model Equation

An IDC has been analytically developed in the theoretical context using partial capacitance and conformal representation [34], suitable for the structure's target capacitance and characteristic impedance. For example, equivalent J-inverter networks, full-wave procedures, and approximate analysis are some adopted techniques. The close-analytical form for determining the unit capacitance per spatial wavelength and the total capacitance, the strip inductance, is equations (1) -(11).

The unit capacitance per cell is denoted by Cu, which is equal to the sum of the equivalent parallel capacitance, C_1, C_2, and C_3 as in equation (1) [24], d is the length of the unit capacitance, L is the total inductance of the structure and the antenna bandwidth (BW) [34], [35].

$$Cu = C_1 + C_2 + C_3 \tag{1}$$

$$C_1 + C_3 = \varepsilon_0 . \frac{(\varepsilon_1 + \varepsilon_3)}{2} . \frac{(K\sqrt{1-k^2})}{K(k)} \tag{2}$$

$$C_2 = \varepsilon_0 \varepsilon_2 \frac{t_m}{S} \tag{3}$$

$$\lambda s = 2(w' + s) = 2d \tag{4}$$

$$C_u = \varepsilon_0 \varepsilon_r \left[\frac{(K\sqrt{1-k^2})}{K(k)} + \frac{t_m}{S}\right]. \tag{5}$$

$$L = 2 \times 10^{-7} l' \left[\text{In}\left(\frac{2l'}{w' + t_m}\right) + \left(0.50049 + \frac{w'}{3l'}\right)\right] \tag{6}$$

$$C = (\varepsilon_r + 1)\, l'[(N-3)Y_1 + Y_2] \tag{7}$$

Where C is the capacitance per unit length, t_m is the thin metal thickness, N is the number of fingers, l and W are the width and length of the structure, and Y_1 and Y_2 defines interior and exterior fingers' capacitance value per unit length and measures in pF/µm. As the lumped structure is finite, the height of the substrate, h, plays a significant role in the IDC performance.

$$Y_1 = 4.409 \tanh\left[0.55\left(\frac{h}{S}\right)^{0.45} \times 10^{-6}\right] \times 10^{-6} \quad (8)$$

$$Y_2 = 9.920 \tanh\left[0.52\left(\frac{h}{S}\right)^{0.50} \times 10^{-6}\right] \times 10^{-6} \quad (9)$$

An overall expression for the total series capacitance of the IDCs can equally be calculated using equations (10) and (11).

$$C_T = \frac{\varepsilon_{re} 10^{-3}}{18\pi} \frac{K(k)}{K'(k)} (N-1) l' \quad \text{(pF)} \quad (10)$$

And,

$$C_T = C_u (N-1) l' \quad (11)$$

In which $K(k)$ and $K'(k)$ is the complete elliptical integral with k-modulus and the complement of the first kind, an effective dielectric constant is ε_{re}, which can be calculated using the finger spacing, S and substrate height h. The ratio of the integral is given by;

$$\frac{K(k)}{K'(k)} = \frac{1}{\pi} \ln\left[2\left(\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)\right], \text{ for } 0.707 \leq k \leq 1 \quad (12)$$

$$\frac{K(k)}{K'(k)} = \frac{\pi}{\ln\left[2\left(\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)\right]}, \text{ for } 0 \leq k \leq 0.707 \quad (13)$$

Moreover, the effective dielectric constant ϵ_{re} is determined by.

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{10h}{w'}\right)^{-\frac{1}{2}} \quad (14)$$

Where an expression for the k and k' are given by

$$k = \frac{s}{d} \quad (15)$$

$$k' = \sqrt{1-k^2} \quad (16)$$

$$BW\ \alpha \sqrt{\frac{L}{C}} \quad (17)$$

3. Results and Discussion

3.1 Experimental Validation

A miniaturized on-chip antenna with enhanced performance is fabricated. The prototype fabrication and the geometrical measurement of the model are shown in Fig 5. The development of the prototype was accomplished using a processed silicon wafer with a thickness of 500µm and a resistivity ranging from 20 to 100 Ω-cm, requiring no additional post-processing. The layer stacking followed the principles of silicon chip development, where metallic pads were incorporated within the SiO_2 layers based on specific targets and limitations, as depicted in Fig. 2. The detailed geometric parameters of the antenna are outlined in Tables 1 and 2. Equally, the fabrication process was conducted from wafer dicing to the sputtering process and finalized at the model prototype, as illustrated in Fig. 4.

Initially, the OCA was simulated using 3D-microwave simulation software to determine key parameters such as gain, radiation characteristics, return loss magnitude, and bandwidth at the operational frequency of 5.8 GHz. Subsequently, a Network Analyzer Agilent (N5245A) was employed to measure the return loss magnitude, as the photograph shows in Fig. 6 (a), yielding values of 23.06 dB and 20.1 dB for the simulated and measured results, as depicted in Fig. 6(b). This resulted in an impedance bandwidth of 0.74 GHz and 0.68 GHz. Fig. 7 illustrates the gain and radiation efficiency with and without the PRS. The introduction of the PRS significantly enhanced peak gain to 2.27 dB and radiation efficiency to 76.8%, compared to the antenna without a PRS, which exhibited a peak gain of 1.62 dB and radiation efficiency of 57.4%.

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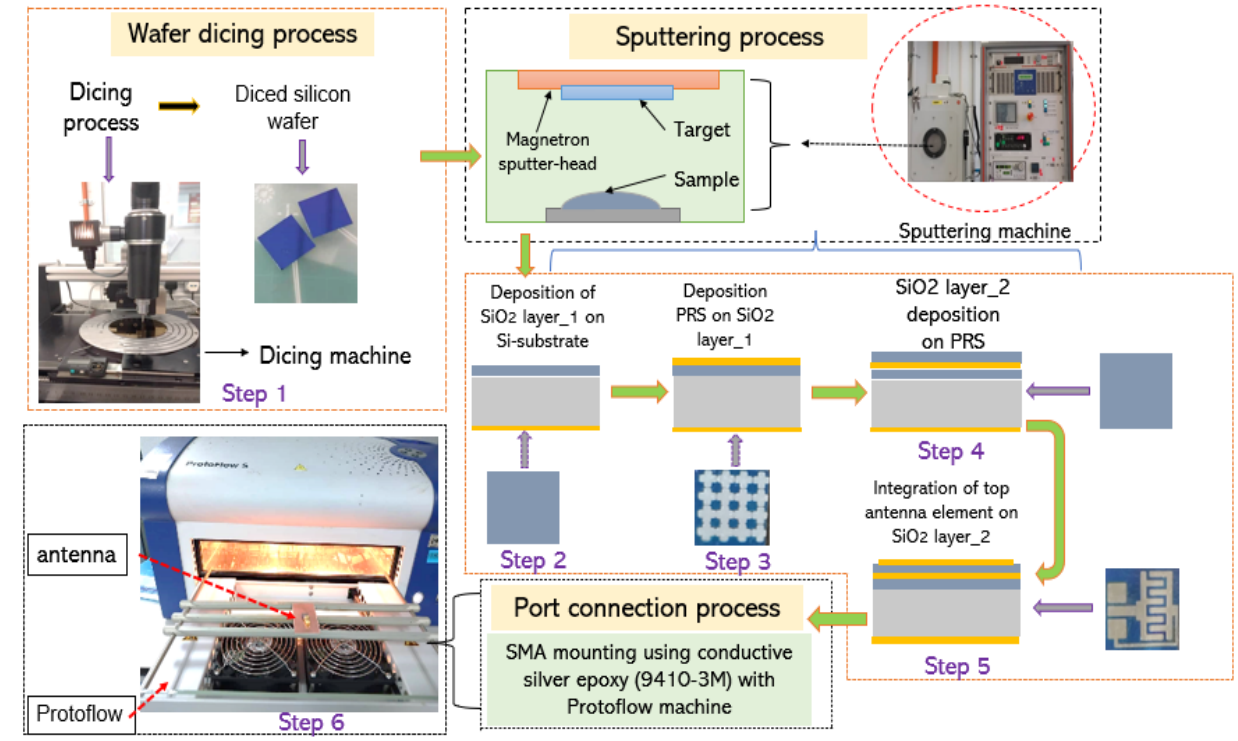
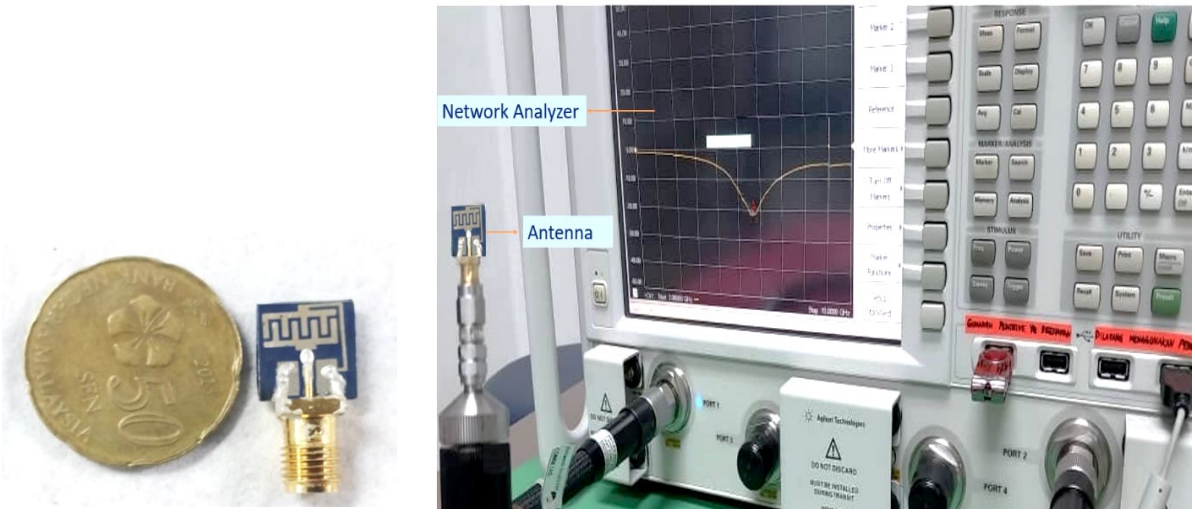
Nevertheless, the measured results indicated a minor deviation in the center frequency towards 5.79 GHz, with a decreased 8% impedance bandwidth compared to the simulated results. This variance could be attributed to the adverse effects of the embedded PRS, which incorporates LC components. Moreover, fabrication tolerances and variations in layer parameters might also contribute to inconsistencies. Conversely, prior discussions have highlighted the PRS's significance in enhancing gain and radiation efficiency within an acceptable range.

Thus, the 2D radiating patterns of the model in both the E—and H-planes were observed at the resonance frequency of 5.8 GHz, as depicted in Fig. 8. The measured input impedance was determined to be 48.92Ω, constituting 97.84% of the 50Ω port impedance. This reveals a mismatch of 2.16%, equivalent to 1.08 Ω, ascribed to the mounting tolerances between the port and the signal PIN due to the utilization of an electrically conductive silver epoxy, HIGH Tg 9410-3M as conventional soldering process was inevitable for silicon material. tolerances between the port and the signal PIN due to using an electrically conductive silver epoxy, HIGH Tg 9410-3M as a conventional soldering process was inevitable for silicon material.



(a)



(b) **(c)**

Fig. 5 *Fabrication and measurement (a) Fabrication process; (b) Fabricated antenna;(c) Measurement set-up*

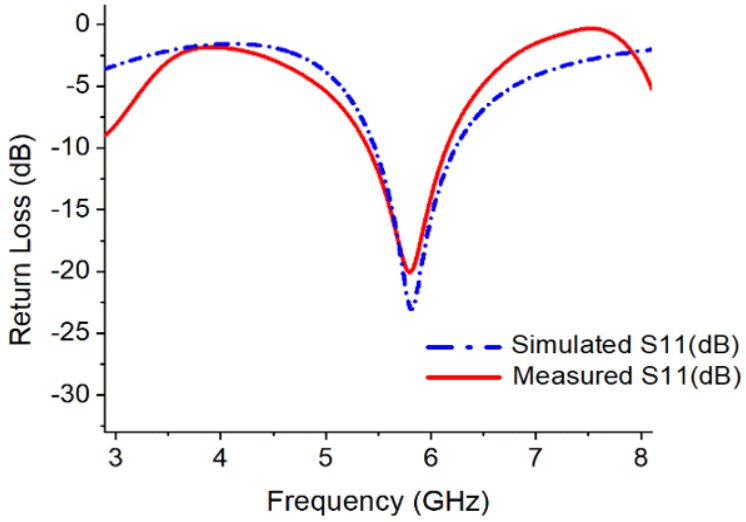
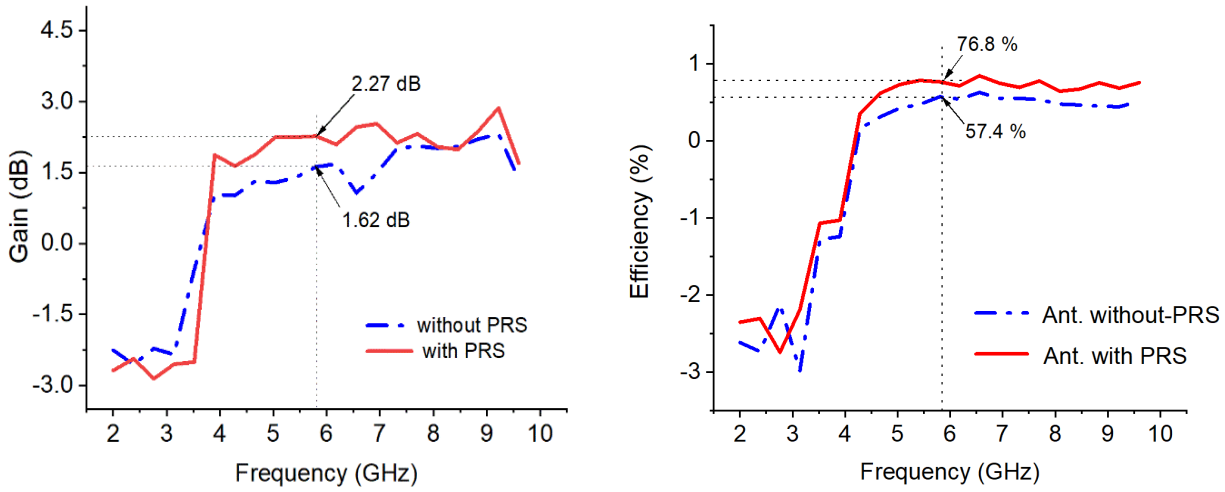
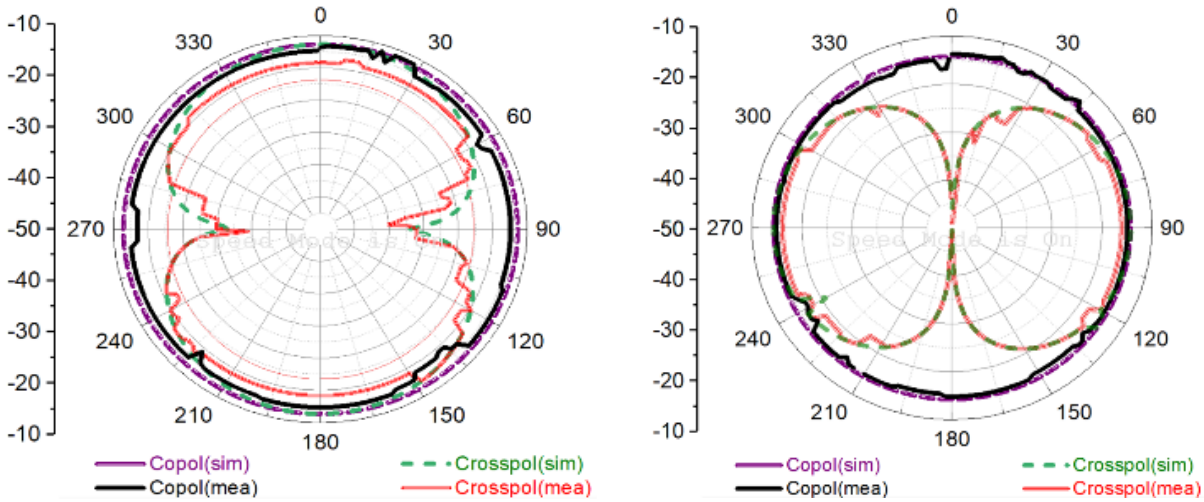


Fig. 6 *Comparison of the simulated and measured magnitude of S11 of the proposed antenna at 5.8 GHz*



(a) **(b)**

Fig. 7 *The gain and radiation efficiency of OCA with- and without- PRS (a) Gain(dB; (b) Radiation efficiency (%) at 5.8 GHz*



(a) **(b)**

Fig. 8 *Absolute simulated and measured 2D radiation pattern at 5.8 GHz (a) E-plane; (b) H-plane*

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3.2 Characteristics of PRS Structure

A PRS unit cell was designed and positioned inside the waveguide ports, with boundary conditions applied to the x- and y-planes. The structure was then analyzed using a frequency domain solver. Thus, reflection and transmission coefficients are obtained, as shown in Fig. 9(a), and the reflection phase at 5.79 GHz is shown in Fig. 9(b). It can be observed from Fig 9(a) that the reflection and the transmission coefficient occurred at -0.208 dB and -24.78 dB over the band frequency of 5.7- 5.9 GHz. Similarly, Fig.9(b) shows that the frequency at 0° reflection phase was realized at 5.79 GHz, which is approximately the center frequency of 5.8 GHz, indicating the good performance of the PRS in EM obstruction. The introduction of PRS offers an insertion loss of 3 dB at transmission poles from 5.52 GHz – 6.25 GHz and below 0.2 dB at the center frequency of 5.79 GHz.

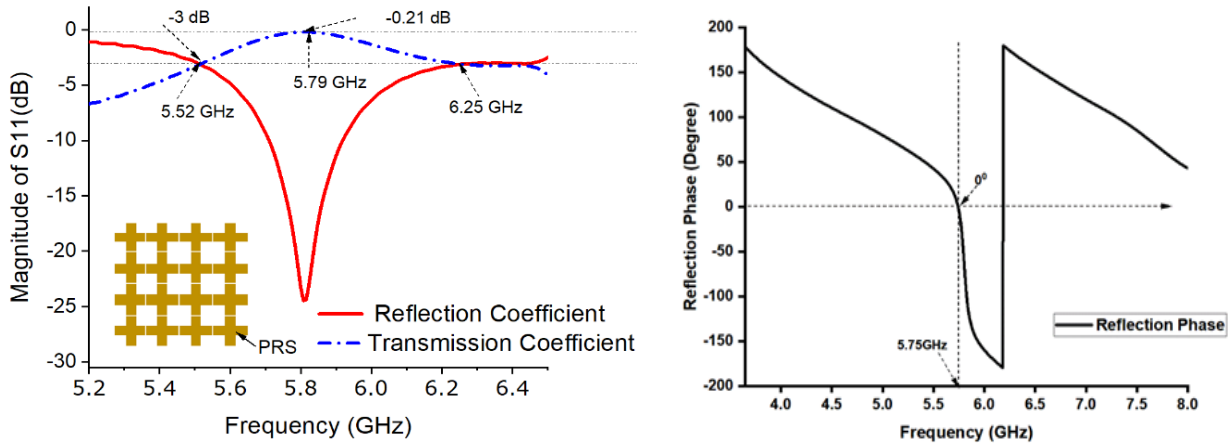

Fig. 9 *Simulated PRS parameters (a) Reflection and transmission coefficient; (b) Reflection phase at 5.8 GHz*

3.3 Effect of Separation Distance 'S' on the Magnitude of S11

The characteristics of IDC are notably influential on both the capacitance and inductance of the component. This portion of the study investigates the impact of the gap distance 's' between the electrodes' fingers. It reveals that altering the 's' value significantly affects the center frequency due to variations in capacitance and inductance. Fig. 10 illustrates the frequency shift as 's' values increase or decrease. This suggests that adjusting the width, W, length *l*, and the 's' of the IDC component can lead to significant frequency shifts since the resonant frequency is inversely related to the total capacitance. This relationship can be expressed as in equation (18).

$$f_R \alpha \frac{1}{\sqrt{C_{eq}}} \tag{18}$$

Where C_{eq} is the total capacitance of the fingers and the adjacent winds, and f_R is the resonance frequency.

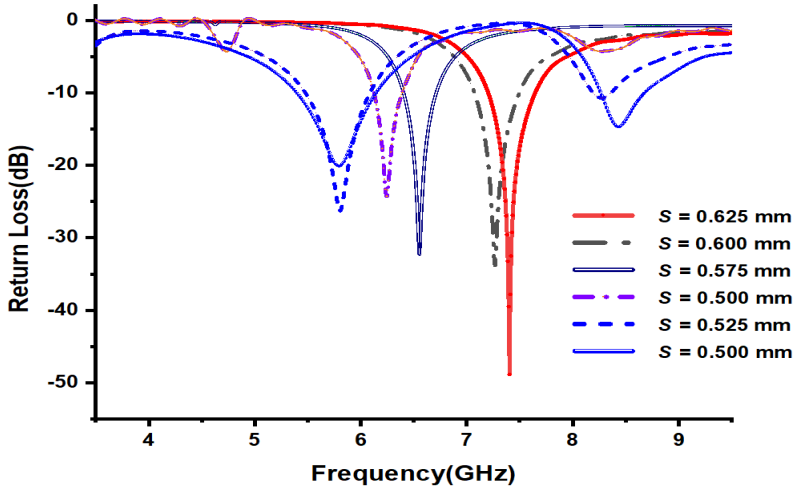

Fig. 10 *Simulated reflection coefficient at different separation distances*

3.4 The Effect of SiO2 Thickness on Antenna Gain

In the design of OCA, variations in the metal density and the thickness of the oxide layers notably influence antenna performance. This study investigates the impact of varying SiO_2 thickness on antenna gain, employing various thicknesses ranging from 0.4 to 2.4µm at intervals of 0.4µm. Simulation results revealed that increasing SiO_2 thickness significantly increased the gap between the top radiating element and the PRS, consequently boosting antenna gain. This enhancement is attributed to the induced capacitance between the PRS and the antenna, fostering mutual coupling and improving the OCA performance. Fig. 11 shows the influence of SiO2 thickness on OCA performance.

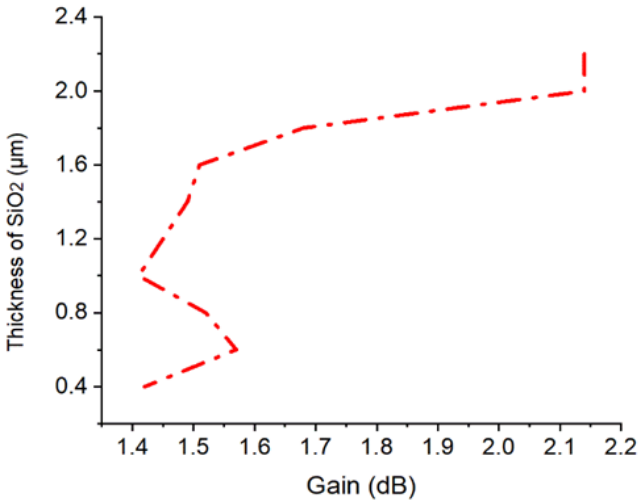

Fig. 11 *The effect of SiO_2 thickness on the antenna gain*

4. Comparison

Table 3 compares the performance of the proposed antenna with the contemporary miniaturized on-chip antennas and their design process. Miniaturized on-chip antennas were realized by adopting a meandered technique with monopole radiator configuration [18], complementary loop-based [37], loop-inspired meander line structure [38] and [39]. All the configurations achieved compact footprint chip size. Conversely, the relatively low gain and radiation efficiency were apart from [38], which realized a considerable efficiency of 60%. However, it incorporated a glass substrate, which possesses low losses due to its reasonable dielectric constant compared to a silicon substrate with 11.7-11.9.

Table 3 *Comparison of proposed work with published work*

Ref	Antenna Type	Freq (GHz)	Size (mm^3)	Max. Gain (dB)	Rad. Eff (%)	Bandwidth (GHz)	Design Process
[18]	Monopole Meandered	9.45	1.6 x 1.9	-29.2	21.07	NM	0.18µm CMOS
[36]	Loop	5.8	1.4 x1.4	-48.93	NM	NM	0.18µm CMOS
[37]	Meandered Loop	5.05	4.0x4.0	NM	60	0.2	Si-wafer+ glass packaging
[38]	Meander Loop	5.8	6.0 x0.5	-40	25	NM	0.13µm CMOS
[39]	Loop	5.8	1.05x 0.85	-23.7		NM	0.18µm CMOS
Proposed work	Monopole planar	5.8	7.25x 3.35	2.27	76.8	0.73	Si-wafer + SiO_2

NM: Not Mentioned, Rad. Eff: radiation Efficiency, Freq. Frequency, Si: Silicon

5. Conclusion

This study reported a miniaturized on-chip antenna design with enhanced gain and radiation characteristics. An IDC was loaded onto a monopole planar radiating conductor as a miniaturization approach, resulting in a compact footprint chip size of 0.14x0.064x0.01$\lambda_o{}^3$. The use of IDC not only impacted the LC components but also controlled the radiation resistance. The design incorporated PRS as a shield for migrating incidence waves and back radiation from the top antenna element into the lossy si substrate. A model prototype was fabricated and measured in an anechoic chamber to validate the design. The results show an increased gain of 28.62%, radiation efficiency of 25.26 %, and the impedance bandwidth of 0.73 GHz. This enabled RFIC, Wi-Max, Wi-Fi 6, and other 5.8 GHz applications. This enhancement ensures additional space and lower power consumption despite the larger electrical wavelength at lower frequencies.

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Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of the paper.

Author Contribution

The authors confirm their contribution to the paper as follows: ***study conception and design:*** *Ahmadu Girgiri, Mohd Fadzil Ain, Mohd Zamir Pakhurddin;* ***data collection:*** *Bello Muhammad Abdullahi; Mohd Nazri Mahmud, Mohd Faiz Mohamed Omar;* ***analysis and interpretation of results:*** *Ahmadu Girgiri, Mohd Faiz Mahamed Omar;* ***draft manuscript preparation:*** *Mohd Fadzil Ain, Ahmadu Girgiri. All authors reviewed the results and approved the final version of the manuscript.*

References

[1] Ikram, M., Sultan, K., Lateef, M. F., & Alqadami, A. S. M. (2022). A Road towards 6G communication- A review of 5G antennas, arrays, and wearable devices. *Electronics*, *11*(10), p. 169. https://doi.org/10.3390/electronics11010169.

[2] Karim, R., Iftikhar, A., Ijaz, B., & Ben Mabrouk. I. (2019). The potentials, challenges, and future directions of on-chip antennas for emerging wireless Applications- A comprehensive survey. *IEEE Access*, 7, pp. 173897–173934, 2019. https://doi.org /10.1109/ACCESS.2019.29573.

[3] Shamim, A., & Zhang, H. (2020). On-chip antenna: challenges and design considerations. In Antennas and Propagation for 5G and Beyond (Eds), (pp. 123–155). Institution of Engineering and Technology. https:// 10.1049/pbte093e_ch6

[4] Jeon, Y., & Koo, J. (2023). Design of front-end receiver and matrix for 2–18 GHz with a searching and tracking function for an ELINT System. *Journal of Electromagnetic Engineering and Science, 23*(1), pp. 38–46. https://doi.org/10.26866/jees.2023.1.r.142

[5] Cheema, H. M., & Shamim, A. (2013). The last barrier: on-chip antennas. *IEEE Microwave Magazine*, *14*(1), pp. 79–91. https:// doi.org/0.1109/MMM.2012.2226542.

[6] Sene, B., Reiter, D., Knapp, H., & Pohl, N. (2022). Design of a cost-efficient monostatic radar sensor with antenna on chip and lens in package. *IEEE Transactions on Microwave Theory and Technology*, *70*(1), pp. 502–512.

[7] Park, Y. J. H., Tran, N. M., Hwang, S. I., Kim, D. I., & Choi, K. W. (2021). Design and Implementation of 5.8 GHz RF Wireless Power Transfer System. *IEEE Access*, *9*, pp. 168520–168534. https://doi.org/ 10.1109/ACCESS.2021.3138221.

[8] De Kok, M., Smolders, A. B., & Johannsen, U. (2021). A review of design and integration technologies for D-Band antennas. *IEEE Open Journal and Antennas Propagation*, *2*, pp. 746–758. https://doi.org/ 10.1109/OJAP.2021.3089052.

[9] Karim, R., Iftikhar, A., & Ramzan, R. (2020). Performance-issues-mitigation-techniques for on-chip-antennas – Recent developments in RF, MMwave, and Thz bands with future directions. *IEEE Access*, *8*, pp. 219577–219610.

[10] Deng, T., & Zhang, Y. P.(2020). *Handbook of Antenna Technologies*. Singapore: Springer Singapore. https://doi.org/10.1007/978-981-4560-75-7.

[11] Sunitha, A., & Manickam, B. (2018). Co-design of on-chip loop antenna and differential class-E power amplifier at 2.4 GHz for biotelemetry applications. *Microelectronics Journal*, *86*, pp. 40–48. https://doi.org/ 10.1016/j.mejo.2019.02.015.

[12] Singh, H., Mandal, S., Mandal, S.K., & Karmakar, A. (2019). Design Of miniaturised meandered loop on-chip antenna with enhanced gain using shorted partially shield layer for communication at 9.45 GHz. *IET Microwaves, Antennas and Propagation.*, *13*(7), pp. 1009–1016. https://doi.org/10.1049/iet-map.2018.5974.

[13] Alibakhshikenari, M., Babaelian, F., Virdee, B. S., Aissa, S., Azpilicueta, L., See, C. H., Althuwayb, A.A., Huynen, I., Abd-Alhammed, R. A., Falcone, F., & Limiti, E. (2020). A comprehensive survey on various decoupling mechanisms with focus on metamaterial and metasurface principles applicable to SAR and MIMO antenna systems. *IEEE Access*, *8,* pp. 192965–193004. https://doi.org/10.1109/ACCESS.2020.3032826.

[14] M. Alibakhshikenari, M., Ali, E., Soruri, M., Dalarsoon, M., Naser-moghadasi, M., Virdee, B. S., Stefanovic, C., P-Dabrowska, A., Kozeil, S., Szczepanski, S., and Limiti, E. (2020). A comprehensive survey of metamaterial transmission-line based antennas: Design, challenges, and applications. *IEEE Access*, *8*, pp. 144778–144808, https://doi.org/10.1109/ACCESS.2020.3013698.

[15] Okabe, K., Lee, W., Harada, Y., & Ishida, M. (2012). Silicon-based On-chip Antenna using an LC Resonator for Near-field RF Systems. *Solid State Electronics.*, *67*(1),pp. 100–104, https://doi.org/10.1016/j.sse.2011.08.002.

[16] Chilukuri, S., & Gundappagari, S. (2020). A wide dual-band metamaterial-loaded antenna for wireless applications. *Journal of Electromagnetic Engineering and Science*, 20(1), pp. 23–30. https://doi.org/10.26866/jees.2020.20.1.23.

[17] Jantarachote, V., Chalermwisutkul, S., Schraml, K., & Heberling, D. (2017). Comparison of meander line and NFRP miniaturization techniques for RFID on-chip antennas. *Proceedings of the 2017 International Symposium on Antennas and Propagation (ISAP)*, pp. 1–2. https://doi.org/10.1109/ISANP.2017.8228986.

[18] Singh, H., & Mandal, S. K. (2020). Miniaturized on-chip meandered loop antenna with improved gain using partially shield layer. *Preceding of the 14th European Conference on Antennas Propagation, EuCAP,* pp. 13–16.

[19] Ghosh, B., S. M. Haque, S.M., Mitra, D., & Ghosh, S. (2010). A loop loading technique for the miniaturization of non-planar and planar antenna. *IEEE Transaction on Antennas and Propagation*, *58*(6) , pp. 2116–2121, 2010. https://doi.org/10.1109/TAP.2010.2046842.

[20] Fallahpour, M., & Zoughi,R. (2018). Antenna Miniaturization Techniques. *IEEE Antennas and Propagation Magazine*, *60* , pp. 38–50.

[21] Kim, S. H., & Jang, J. H. (2010). Compact folded monopole antenna with LC-loadings. In *International Workshop on Antenna Technology*, Lisbon, Portugal.

[22] Wang, M., Tang, M., Zhang, L.P., Zhang, H.C., Xu, J., Cui, T. J., & Ma, J. (2021). Miniaturization of frequency-reconfigurable antenna using periodic slow-wave Structure. *IEEE Transactions on Antennas and Propagation*, *69*(11), pp.7889–7894.

[23] Ud Din, I., Ullah, W., Abaashi, N. A., Ullah, S., Shihzad, W., Khan, B., & Jayakodi, D. N. K. (2023). A Novel compact ultra-wideband frequency selective surface-based antenna for Gain enhancement applications. *Journal of Electromagnetic Engineering and Science*, *23*(2), pp.188–201. https://doi.org/10.26866/jees.2023.2.r.159.

[24] Rachmanita, R. E., Muntini, M. S., Thawankaew, S., Chao-Moo, W., Vora-Ud, A., & Seetawan, T. (20181). Fabrication and characterization of interdigital capacitors thin film by DC magnetron sputtering for measuring the permittivity of crude oil. *Material Today-Proceedings*,5(7),pp.1519215197.https://doi.org/10.1016/j.matpr.2018.04.081.

[25] Falk, H. (2004). Interdigital Sensors and Transducers. *Proceeding of the IEEE*, *92*(5), pp. 806–807. https://doi.org/10.1109/jproc.2004.826604.

[26] Kushwaha, R. K., Karuppanan, P., & Dewang, R. K. (2020). Design of a SIW on-chip antenna using 0.18-μm CMOS process technology at 0.4 THz. *Optik (Stuttg)*, *223, no.*165509. https://doi.org/10.1016/j.ijleo.2020.165509.

[27] Liu, Q., Van den Biggelaar, A. J., Johannsen, U., Van Beurden, M. C., & Smolders, A. B. (2020). On-chip metal tiling for improving grounded mm-wave antenna-on-chip performance in standard low-cost packaging. *IEEE Transaction on Antennas and Propagation*, *68*(4), pp. 2638–2645. https://doi.org/10.1109/TAP.2019.2957713.

[28] Sinha, S., Libois, M., Vaesen, K., Suys, H., Pauwels, L., & Ocket, I. (2021). Miniaturized (127 to 154) GHz dipole arrays in 28 nm bulk CMOS with enhanced efficiency. *IEEE Transaction on Antennas and Propagation*, *69*(3), pp. 1414–1426.

[29] Olokede, S. S., Okonkwo, C. J., Akinyemi, A. T., & Paul, B. S. (2018). A novel miniaturized quasi-lumped element antenna based on interdigital capacitor," *At 2018 Progress in Electromagnetic Research. Symposium, Toyam*a, Japan.

[30] Ain, M. F., Olokede, S. S., Qasaymeh, Y. M., Marzukia, A., Mohammed, J. J., Sreekantan, S., Hutagalung, S. D., Ahmad, Z. A., & Abdulla, M. Z. (2013). A novel 5.8 GHz quasi-lumped element resonator antenna. *International Journal of Electronics and Communications (AEÜ)*, *67*(7), pp. 557-563. https://doi.org/10.1016/j.aeue.2012

[31] Li, R., Qu, L., Shin, S., Lee, H., Wi, S., Kim, J., & Kim, H. (2024). Impedance bandwidth enhancement using capacitor-controlled series resonance in an antenna's feeding structure. *Journal of Electromagnetic Engineering and Science, 24*(2), pp. 129–137. https://doi.org/10.26866/jees.2024.2.r.212.

[32] Liu, C. C., & Rojas, R. G. (2016). V-band integrated on-chip antenna implemented with a partially reflective surface in standard 0.13-μm BiCMOS technology. *IEEE Transactions on Antennas and Propagation*, *64*(12), pp. 5102–5109. https://doi.org/10.1109/TAP.2016.2620606.

[33] Nafe, M., Syed, A., & Shamim, A. (2017). Gain-enhanced on-chip folded dipole antenna utilizing artificial magnetic conductor at 94 GHz. *IEEE Antennas and Wireless Propagation Letters*, *16*, pp. 2844–2847. https://doi.org/10.1109/LAWP.2017.2749308.

[34] Bahl, I. (2003). *Lumped Elements for RF and Microwave Circuits*, *4*(1), pp. 88-100, Boston, London.

[35] Kamal, S., Mohammed, S. B. AM., Ain, M. F., Ullah, U., Hussin, R., Ahmad, Z. A., Othman, M., & Ab Rahman,M. F., (2020). A novel lumped LC resonator antenna with air-substrate for 5G mobile terminals. *Progress in Electromagnetic Research Letters*, *88*, pp. 75–81. https://doi.org/10.2528/pierl19090509.

[36] Razak, A. H. A., Shamsuddin, M. I. A., Idros, M. F. M., Halim, A. K., Ahmad, A., & Junid, S. A. M. A. (2018). Design of 5.8 GHz Integrated Antenna on 180nm Complementary Metal-Oxide Semiconductor (CMOS) Technology. *IOP Conference Series:. Material Science and Engineering*, Kuchick Sarawak, Malaysia, 2018.

[37] Mendes, P. M., Polyakov, A., Bartek, M., Burghartz, J. N., & Correia, J. H. (2006) "Integrated chip-size antennas for wireless microsystems: Fabrication and design considerations*", Sensors and Actuators A,* vol. 125, no. 2, pp.217–222. 2006. doi: 10.1016/j.sna.2005.07.01

[38] Lin. J., Wu, H., Su, Y., Gao, L., Sugavanam, A., Brewer, J. E., & Kenneth, K. O. (2007). Communication using antennas fabricated in silicon integrated circuits. *IEEE Journal of Solid-State Circuits, 42*(8), pp.1678-1687.

[39] Charlot, E., Hamada, M., & Kuroda, T. (2021). An on-chip antenna with an area of 0.9 square millimeters for RFID applications in the 5.8 GHz - 24 GHz range. *Preceding of the 2020 International Symposium on Antennas Propagation, ISAP 2020*. https://doi.org/10.23919/ISAP47053.2021.9391369.