INTERNATIONAL JOURNAL OF INTEGRATED ENGINEERING
ISSN: 2229-838X e-ISSN: 2600-7916

IJIE

Vol. 17 No. 1 (2025) 381-391
https://publisher.uthm.edu.my/ojs/index.php/ijie

Design of High Efficiency Class E Power Amplifier Utilizing 0.18-µm RF CMOS Technology for 5G Network

Sohiful Anuar Zainol Murad[1]*, Ahmad Fariz Hasan[1,2]

1. *Centre of Excellence for Micro System Technology (MiCTEC), Universiti Malaysia Perlis (UniMAP), 02600 Arau, Perlis, MALAYSIA*
2. *Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis (UniMAP), 02600 Arau, Perlis, MALAYSIA*

*Corresponding Author: sohiful@unimap.edu.my
DOI: https://doi.org/10.30880/ijie.2025.17.01.031

Article Info

Received: 12 August 2024
Accepted: 4 November 2024
Available online: 30 April 2025

Keywords

Power amplifier, radio frequency, CMOS, PAE, two stage

Abstract

The design of high-efficiency class E power amplifiers faces challenges due to low transistor breakdown voltages, high parasitic capacitances, and limited quality of on-chip passive components, which reduce power efficiency and linearity. Existing solutions offer moderate efficiencies but often require complex trade-offs that are not ideal for high-frequency applications. This research aims to optimize a class E power amplifier design to achieve higher efficiency and output power for 5G newtork, addressing these limitations while maintaining performance suitable for modern wireless communication systems. This paper proposed a high efficiency class E PA for 5G network. The proposed PA is implemented using the 0.18-µm RF CMOS process technology, and the circuit is designed and simulated using Cadence software. The proposed PA consists of a power stage and a driver stage. The power stage and the driver share a single source. The simulation results show that at input power of 0 dBm and supply voltage of 1.8 V, the proposed PA demonstrates a maximum peak power added efficiency (PAE) of 55 %. Meanwhile, a maximum output power (Pout) of 13.1 dBm is delivered by the proposed PA. Since the PA exhibits a stability factor (K value > 1), it is unconditionally stable. In addition, the PA achieves s-parameter of S11, S22 and S21 performances of -13.8 dB, -29.3 dB and 19.7dB, respectively. Furthermore, the layout of the proposed PA is 1.82 mm^2 including the pads.

1. Introduction

Recently, the demand for multimedia material downloads, the use of smart devices, and the number of users have all greatly increased. Fourth Generation (4G) technology as it is currently used can no longer support this growth as mobile customers demand more dependable and quick service [1]. Mobile services, the Internet of Things (IoT), self-driving cars, and smart cities will all be impacted by this technology [2]. As a result, new result
new technologies are currently being created with the goal of creating Fifth Generation (5G) devices. The goal of 5G technology is to deliver 100x more capacity, data rates of up to 1Gb/sec, end-to-end latency of less than 1ms, better Quality of Service (QoS), and massive device connectivity [3–4]. Due to current consumers' high data consumption, the radio frequency (RF) band currently in use by service providers is congested [5]. As a result, mobile services will utilise a new spectrum for the first time thanks to 5G technology.

In Malaysia, the working spectrum bands for 5G ("5G pioneer bands") systems are 700 MHz, 3.4 GHz to 3.8 GHz ("3.5 GHz band") and 24.9 GHz to 28.1 GHz ("26/28GHz bands") [6-7]. Additionally, many nations worldwide have designated a high frequency range of 28 GHz and a low frequency band of 3.5 GHz for use in 5G applications

[8]. Therefore, to satisfy the needs of the 5G network, the current mobile communication transceiver must be changed. The transmitter system's crucial component, the RF power amplifier, is intended to deliver the required power with excellent gain and great efficiency [9]. To obtain a trustworthy transmission, the power amplifier's output power must be adequate. The performance of the RF power amplifier directly affects the effectiveness of the entire system because it is the component in radio transmitters and transceivers that consumes the most power. Therefore, the RF system needs to be well-designed in order to match the 5G need.

The implementation of 5G communication systems is possible in both high band and sub-6 GHz frequency ranges. The concentration of the high frequency band, primarily in the millimeter (mm)-wave region, makes it difficult to implement the radio frequency (RF) terminal [10]. The sub-6 GHz band seems more practical because it can be used with existing base stations and presents fewer design difficulties. Most countries employ the sub-6 GHz major test frequency band between 3.4 and 3.8 GHz. The RF device's low insertion loss in this frequency range significantly increases the transmission power of the terminal.

The design and production of power amplifiers typically makes use of III-V compound semiconductors like GaAs, GaN, and InP. These materials' power amplifiers outperform Si CMOS technology in terms of power output capability and efficiency [11]. When compared to other technologies, the performance of the power amplifier based on Si CMOS technology is the lowest. Furthermore, integrating the complete transceiver onto a single chip becomes more challenging because to the substrate coupling and substrate loss issues with Si CMOS transistors [11]. Si CMOS power amplifiers, however, have the lowest power consumption, maximum integration level, and lowest fabrication cost when compared to other technologies [12].

Table 1compares four key semiconductor technologies for power amplifiers in 5G systems based on their frequency range, efficiency, gain, output power and key features. Gallium Nitride (GaN) operates between 67-100 GHz with moderate efficiency of 7-27% and gain of 6-18 dB, offering high power density and excellent thermal performance, making it suitable for high-frequency applications [13]. Silicon Germanium (SiGe) covers 4-50 GHz, providing good RF performance with higher efficiency of 13-40% and gain of 6-30 dB at a lower cost than GaN, ideal for mid-range frequencies [14]. RF CMOS is optimized for low-frequency bands 2.4-5 GHz, achieving high efficiency of 27-70% and output power of 15-30 dBm, benefiting applications requiring integration with digital circuits [15]. Indium Phosphide (InP) supports ultra-high frequencies (140-255 GHz) with low efficiency of 5-17% and output power of 12-22 dBm, ideal for applications demanding ultra-high-frequency performance and high efficiency [16]. These technologies illustrate the trade-offs in performance characteristics required to meet diverse 5G system demands.

Table 1 *A current advancements of power amplifiers (PAs) for 5G systems*

Technology	Frequency Range (GHz)	Efficiency (%)	Gain (dB)	Output Power (dBm)	Key Features
GaN (Gallium Nitride)	67-100	7-27	6-18	N/A	High power density, excellent thermal performance
SiGe (Silicon Germanium)	4-50	13-40	6-30	N/A	Good RF performance, lower cost than GaN
RF CMOS	2.4-5	27-70	N/A	15-30	High integration with digital circuits, lower power output
InP (Indium Phosphide)	140-255	5-17	N/A	12-22	Ultra-high-frequency performance, very high efficiency

An example of a recent patent related to power amplifiers for 5G systems is China Patent No. CN116888888A, titled high efficiency dual drive power amplifier for high reliability applications. This patent described dual-drive power amplifier (PA) features a differential pair of transistors, M1 and M2, driven by a coupling network with two transmission line couplers. This design enables the input signal to drive both the gate and source terminals of the transistors, allowing the source terminal to go below ground potential. The PA also includes input matching networks, drivers, inter-stage matching networks, and output networks for practical implementation.

2. Design Implementation

A driver stage and a power stage are both included in the two-stage topology of the proposed class E CMOS PA. To achieve a reasonable power gain and efficiency, the suggested PA employs numerous stages. The 0.18-µm CMOS process technology is used in the design of the proposed PA. The proposed PA's schematic is shown in Figure 1.

Int. Journal of Integrated Engineering Vol. 17 No. 1 (2025) p. 381-391

As compared to the previous works, the use of current reuse can lead to increased circuit complexity and may introduce a distortion due to the shared current paths between different stages, potentially degrading the amplifier's linearity and overall signal integrity [17][19]. Reverse body biasing, on the other hand, increases the threshold voltage of MOSFETs, which can reduce the transconductance and thereby lower the gain of the amplifier. This technique also increases the risk of latch-up and leakage currents, especially in deep submicron technologies, which can negatively affect reliability and power efficiency [18]. Therefore, the PA as depicted in Figure 1 is proposed to increase efficiency and reduce circuit complexity. The input stage is made up of a driver stage that is intended to give the second stage enough input signal for high efficiency. A power stage makes up the second stage in the meantime. In order to reduce power loss and achieve high efficiency, the power stage, which comprises a class E amplifier is used.

Single stage common source transistor configurations are used in both the driver stage and the power stage. The transistor size is determined based on I-V characteristics of the NMOS transistor. As the transistor size changes, the proper bias point can be chosen by looking at the amount of current from the Id-Vgs curve. This makes possible to pick a bias point, Vgs. In the saturation region, the drain current, Id, depends on the gate bias voltage, Vgs, and the W/L ratio of the transistor as given in equation (1).

$$I_d = k' \frac{W}{L}[(V_{gs} - V_t)V_{(dsat)} - \frac{V_{dsat}^2}{2}] \tag{1}$$

The M1 NMOS transistor, with a W/L of 224 µm / 0.18 µm, is part of the driver stage. The supply voltage is set to 1.8 V. For the sake of circuit simplicity, the input matching comprises of the DC block capacitors C1 and L1. The input matching is given by:

$$Z_{in} = j\omega L_1 + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_{gs1}} \tag{2}$$

The driver stage's biasing voltage is set to 0.7 V. To give the power stage high gain, the interstage matching network includes series capacitor C2 with a value of 3.7 pF. At the power stage, class E PA is used. A basic inductor called L3 serves as an RF choke, which is used to block radio frequencies (AC current) while allowing DC current to flow through it. A common source power amplifier is used in the power stage. To lower the switch turn-on resistance, a switch transistor of the largest possible size is chosen. The NMOS transistor has a minimum length of 0.18 µm and a width of 7 µm with 32 fingers. The biasing voltage of 0.6 V is chosen at the gate of transistor M2. The voltage supply VDD for transistor M2 is set to 1.8 V. The component values for the proposed power amplifier circuit are shown in Table 2. All the values of capacitors and inductors are chosen to set the resonance at the desired frequency of 3.5 GHz, which is typically can be calculated by $f_o = \frac{1}{2\pi\sqrt{LC}}$.

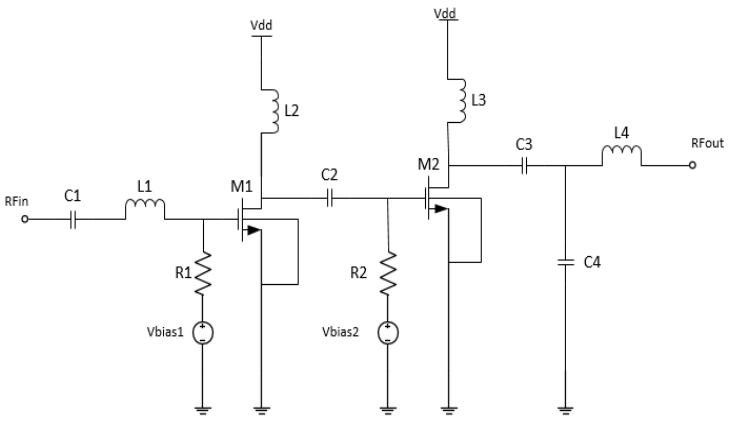

Fig. 1 *The proposed 3.5 GHz CMOS class E PA schematic*

Table 2 *Components value for the proposed PA*

Component	Value
C1	434.8 fF
L1	7.6 nH
R1	467.6 Ω
L2	4.2 nH
C2	3.7 pF
R2	467.6 Ω
L3	4.2 nH
C3	23 pF
C4	362.7 fF
L4	2.3 nH

3. Results And Discussion

The proposed class E CMOS PA is designed and simulated using Cadence Virtuoso software. All the components in the schematic utilize CMOS 0.18-µm technology. The results and analysis are shown in the following section.

3.1 S-parameter

Scattering parameters (S-parameters), are a group of variables used to explain how power amplifiers behave. S-parameters are useful for designing and analyzing RF power amplifiers to determine the gain, impedance matching, and signal loss within these high-frequency systems. Impedance matching is used to maximize power delivery from the source to the load and minimize reflected power loss. Since most RF systems are built around this impedance, a module's input and output impedances typically need to be converted to a common resistance of 50 Ω. The power that is reflected after being transmitted from the source at the input determines the input return loss. When transmitting, there should ideally be no power reflection at the input.

The input return loss (S11) and output return loss (S22) are depicted in Figure 2. The S11 and S22 at 3.5 GHz frequency are -13.8 dB and -29.3, respectively. Because the input and output return losses are kept at -10 dB, the reflected signals won't affect the transmitted signal. The insertion loss is unaffected by the return loss as long as it is less than -10 dB.

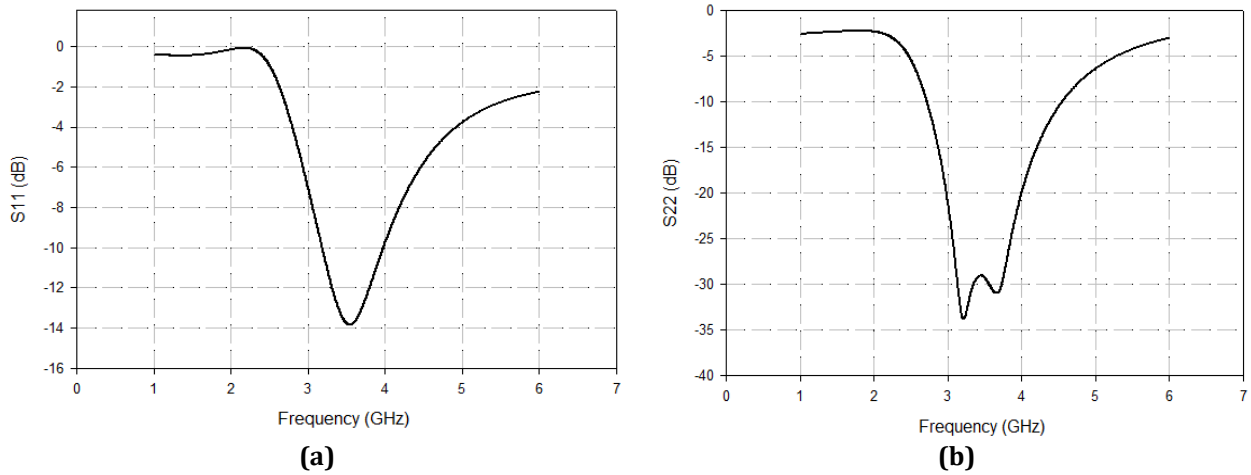

Fig. 2 *The Input and output insertion loss (a) S11; (b) S22*

The ratio of output voltage to input voltage is known as the circuit's gain, sometimes referred to as the forward transmission coefficient. In the s-parameter, the gain is measured using S21. Figure 3 shows the gain of the proposed PA. The proposed PA gain of 19.7 dB is realized at the operating frequency of 3.5 GHz, according to the

Int. Journal of Integrated Engineering Vol. 17 No. 1 (2025) p. 381-391

simulation results. However, the peak of gain is at 2.8 GHz which shifted to the left due to the parasitic effect. Since the input and output impedance are matched at 50 Ω, the peak gain is not optimized at targeted frequency.

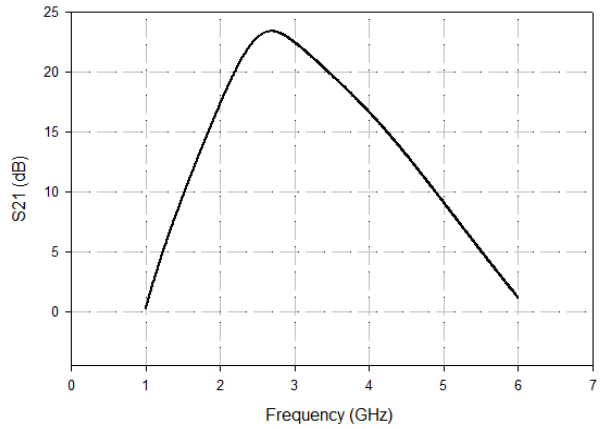

Fig. 3 *Gain of the proposed PA (S21)*

3.2 Power Gain

The ratio of an amplifier's output power to its input power is referred to as amplifier power gain. It measures how well the amplifier boosts the signal's power when supplied to its input. As it reveals the device's capacity for amplification, power gain is a crucial metric in the design and study of amplifiers. The power gain of the proposed PA configuration is shown in Figure 4. As can be seen, when the input power is changed from -30 dBm to -10 dBm, the proposed PA achieves a power increase of 20 dB. When an input larger than -10 dBm is applied, the gain is rolled off.

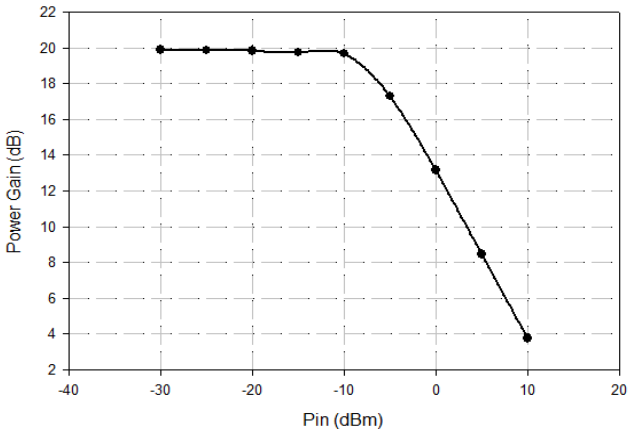

Fig. 4 *Power gain of the proposed PA*

3.3 Power Added Efficiency

The simulated result for PAE at the frequency of 3.5 GHz is presented in Figure 5. As can be seen, that the maximum peak simulated PAE achieved by the proposed power amplifier is 55 % with an input power of 0 dBm at a 1.8 V power supply. Low operating voltage and low dc current flowing through the circuit enable this two stage CMOS power amplifier to operate with high PAE. DC power consumption can be decreased to increase battery life by enhancing the PAE of the power amplifier. In many applications, power amplifiers with a high PAE are crucial because they significantly lower power consumption and mitigate power loss. According to theory, PAE would rise as input power rose. However, when the input power is above 0 dBm, the PAE begins to fall, indicating that the signal is clipping and the PA is being saturated. Due to the parasitic's impacts, the PAE is deteriorating.

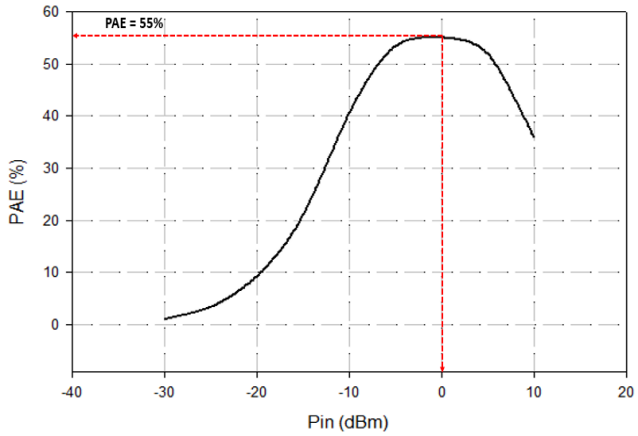

Fig. 5 *Power added efficiency of the proposed PA*

3.4 Stability

In power amplifiers, stability can refer to the ability of the amplifier to maintain its performance characteristics, particularly under varying load conditions. Unstable power amplifiers can exhibit issues like oscillations, distortion, or even damage to the amplifier or connected devices. It is defined as:

$$K_f = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \tag{3}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. Figure 6 represents the simulated result for the stability factor Kf. The stability factor Kf is greater than 1 for the entire frequency range. Therefore, the proposed PA is unconditional stable.

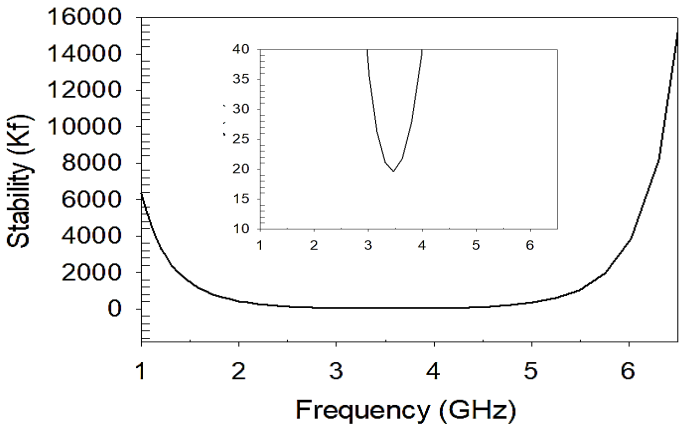

Fig. 6 *Simulated K Factor (Kf) for stability*

3.5 Linearity

The 1 dB gain compression point describes power amplifier saturation. A constant gain is maintained by an amplifier for low-level input signals. At greater input levels, the power amplifier, however, saturates and loses gain. The 1 dB gain compression point (P1dB) is the power level at which the gain is reduced by 1 dB from its small signal value. The P1dB is calculated using the gain relationship between the input power and output power. Figure 7 shows an output power against input power graph. The output power and saturated output power of the power amplifier are 12.1 dBm and 13.1 dBm, respectively, at a 1 dB compression point. According to Figure 7, the input power of -5.5 dBm is where the 1 dB compression point is located.

Int. Journal of Integrated Engineering Vol. 17 No. 1 (2025) p. 381-391

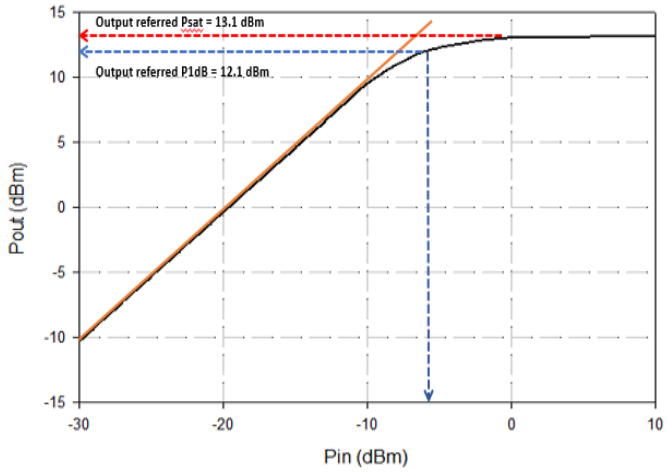

Fig. 7 *Simulated P1dB at 3.5 GHz*

3.6 Relationship between output power and efficiency

Output power and PAE are plotted against supply voltage is shown in Figure 8. When the supply voltage is swept from 1.0 to 2.2 V, the output power increases from 8 dBm to 14.7 dBm in a manner that is roughly proportional to VDD. The supply voltage can be used to regulate the output power based on the outcome. It is also possible to observe that PAE varies roughly proportionately to voltage when the voltage is swept from 1.0 to 1.8 V. The PAE starts to saturate when a high supply voltage is used, which is greater than 2 V. As soon as the PA achieves saturation, the PAE decreases. The plot indicates that the maximum PAE occurs at a supply voltage of 2 V.

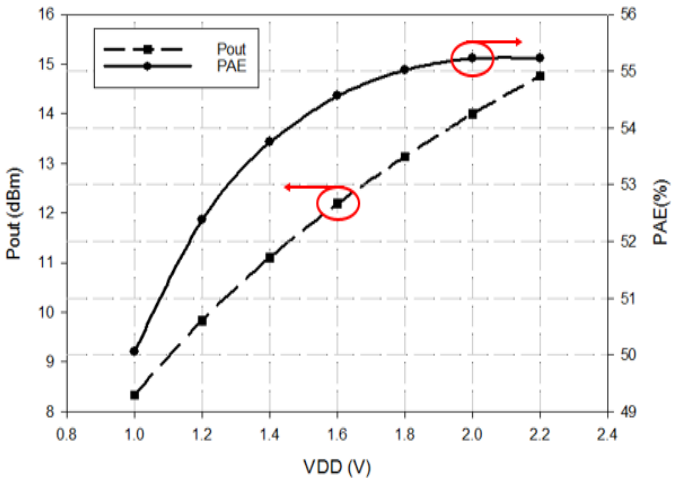

Fig. 8 *Output power and PAE versus supply voltage*

Figure 9 depicts the plot of output power and PAE as a function of frequency. The output power is kept at least at 13 dBm across the frequency range of 2.5 to 3.6 GHz. The highest output power is achieved at a frequency of 2.8 GHz. Furthermore, a high efficiency of more than 55 % can be achieved in the frequency range of 3.0 to 3.5 GHz. As a result, this PA can perform better at frequencies ranging from 3.0 to 3.5 GHz. The plot shows that the highest PAE is achieved when the frequency is 3.2 GHz.

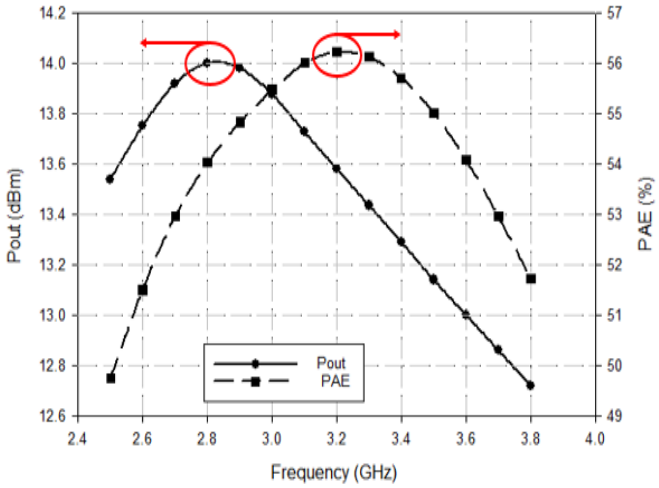

Fig. 9 *Output power and PAE versus frequency*

3.7 Layout

The design of the proposed CMOS power amplifier is shown in Figure 10. Utilizing 0.18-m RF CMOS technology, Virtuoso Layout Editor is used to create the proposed PA's layout. Including the pads, the implemented PA chip occupied 1.43 mm × 1.27 mm of die area. Inductors, capacitors, and MOS transistors make up the layout's primary modules. For the proposed PA, NMOS transistors are preferred because of the better performance due to the higher mobility of electrons versus holes. The dimensions of the NMOS transistors are W/L = 224µm/0.18µm. Metal-Insulator-Metal (MIM) capacitors were used in the matching networks of this PA design. The polysilicon gate resistors are used for gate bias in the NMOS transistors. As can be seen in Figure 10, hexagonal spiral inductors were employed in the proposed PA design. On-chip inductors are frequently the largest passive components in RF systems and play an important role in performance. The restrictions on other design factors will be greatly loosened by good inductors. The spiral inductor is essential because it is the performance limiting component in the PA. The resistive losses in the spiral coil and the substrate losses limit the inductors' quality factor (Q). High quality inductors are challenging to build in bulk CMOS due to parasitic losses. As a result, creating on-chip inductors with higher quality factors in RF CMOS processes is possible using a larger top metal layer.

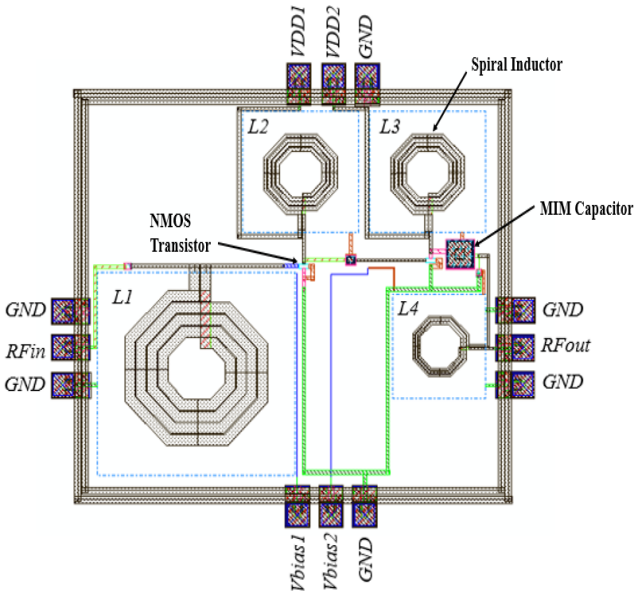

Fig. 10 *Layout of the proposed PA utilizing 0.18-µm RF CMOS technology*

Table 3 presents a performance summary of CMOS power amplifiers (PAs) for 5G networks, comparing with previously published works. The current work, utilizing a 180 nm technology node at 3.5 GHz with a supply voltage of 1.8 V, achieves a PAE of 55% and an output power of 13.1 dBm, with a chip size of 1.82 mm^2. This PAE is higher than that of similar works, such as [19] which achieved 43.9% PAE at a similar frequency and output power using a 130 nm technology node, and [21], which demonstrated a lower PAE of 36.9% with a 45 nm process but at a reduced output power of 6.8 dBm. Additionally, the chip size of the current work is larger than most, except for [19], indicating a trade-off between efficiency and integration density. Overall, the results suggest that the current work provides a notable improvement in efficiency while maintaining competitive output power and demonstrates effective performance suitable for 5G applications.

Table 3 *Performance summary of CMOS PA*

Reference	Technology (nm)	Frequency (GHz)	V_{DD} (V)	PAE (%)	Pout (dBm)	Chip Size (mm^2)
[17]	130	3.5	1.8	50.5	13	0.78
[18]	180	3.5	1.8	54.6	8.2	N/A
[19]	130	3.5	1.8	43.9	13.5	1.47
[20]	130	2.4	1.2	40.6	17.6	0.11
[21]	45	3.5	1.0	36.9	6.8	0.21
[22]	130	2.4	2.0	46	17.3	1.05
This work	180	3.5	1.8	55.0	13.1	1.82

Conclusion

This work uses a 0.18-m RF CMOS process to offer a 3.5 GHz CMOS PA. The driver stage and the power stage are two phases that are part of the design PA. Both stages utilize a single stage common source transistor design. The proposed class E power amplifier (PA) demonstrates several advantages that make it well-suited for 5G network applications. It achieves a high peak power added efficiency (PAE) of 55%, indicating strong energy efficiency, and delivers a maximum output power of 13.1 dBm, ensuring robust signal transmission. The PA is unconditionally stable, with a stability factor (K value > 1), which ensures reliable performance across various operating conditions. Its compact design, occupying just 1.82 mm^2, is ideal for integration into small, modern devices. Optimized using 0.18-µm RF CMOS technology, the PA is designed for high-frequency 5G applications, and its excellent S-parameter performance ensures good input and output matching, reducing signal reflection and maintaining signal integrity.

Acknowledgement

The author would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) under a grant number of FRGS/1/2020/TK0/UNIMAP/02/26 from the Ministry of Higher Education Malaysia. Special thanks to Nur Sakinah Mohd Yunus for her contributions to simulation and results analysis.

Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The authors confirm contribution to the paper as follows: ***power amplifier design and simulation:*** *Sohiful Anuar Zainol Murad;* ***analysis and interpretation of results:*** *Ahmad Fariz Hasan;* ***draft manuscript preparation:*** *Sohiful Anuar Zainol Murad, Ahmad Fariz Hasan. All authors reviewed the results and approved the final version of the manuscript.*

References

[1] Agiwal, M., Roy, A., & Saxena, N. (2016). Next generation 5G wireless networks: A comprehensive survey. *IEEE communications surveys & tutorials*, 18(3), 1617-1655. https://doi.org/10.1109/COMST.2016.2532458

[2] Elsayed, N., Saleh, H., Mohammad, B., & Ismail, M. (2017, December). Doherty CMOS power amplifiers for 5G technology. *In 2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)* (pp. 34-37). IEEE. https://doi.org/10.1109/ICECS.2017.8292114

[3] Asbeck, P. M. (2016, May). Will Doherty continue to rule for 5G? *In 2016 IEEE MTT-S International Microwave Symposium (IMS)* (pp. 1-4). IEEE. https://doi.org/10.1109/MWSYM.2016.7540208

[4] Adebusola, J. A., Ariyo, A. A., Elisha, O. A., Olubunmi, A. M., & Julius, O. O. (2020, March). An overview of 5G technology. *In 2020 international conference in mathematics, computer engineering and computer science (ICMCECS)* (pp. 1-4). IEEE. https://doi.org/10.1109/ICMCECS47690.2020.240853

[5] Gupta, A., & Jha, R. K. (2015). A survey of 5G network: Architecture and emerging technologies. *IEEE access, 3, 1206-1232*. https://doi.org/10.1109/ACCESS.2015.2461602

[6] Yi, K. S., Murad, S. A. Z., & Mohyar, S. N. (2021, July). Design of 2.4 GHz Two Stages Cascode Class E Power Amplifier for Wireless Application. In *Journal of Physics: Conference Series (Vol. 1962, No. 1, p. 012017). IOP Publishing.* https://doi.org/10.1088/1742-6596/1962/1/012017

[7] Hasan, A. F., Murad, S. A. Z., Bakar, F. A., & Zulkifli, T. Z. A. (2020). A 28 GHz high efficiency fully integrated 0.18 µm combined CMOS power amplifier using power divider technique for 5G millimeter-wave applications. *Bulletin of Electrical Engineering and Informatics, 9(2), 644-651*. https://doi.org/10.11591/eei.v9i2.1854

[8] Shayea, I., Azmi, M. H., Ergen, M., El-Saleh, A. A., Han, C. T., Arsad, A., ... & Nandi, D. (2021). Performance analysis of mobile broadband networks with 5g trends and beyond: Urban areas scope in malaysia. *IEEE Access, 9, 90767-90794.* https://doi.org/10.1109/ACCESS.2021.3085782

[9] Yuan, H., Zhou, R., Wang, P., Xu, H., & Wang, Y. (2023). A 55 nm CMOS RF Transmitter Front-End with an Active Mixer and a Class-E Power Amplifier for 433 MHz ISM Band Applications. *Electronics*, 12(22), 4711. https://doi.org/10.3390/electronics12224711

[10] Akyildiz, I. F., Han, C., & Nie, S. (2018). Combating the distance problem in the millimeter wave and terahertz frequency bands. *IEEE Communications Magazine,* 56(6), 102-108. https://doi.org/10.1109/MCOM.2018.1700928

[11] Wang, Z., Hu, S., Gu, L., & Lin, L. (2022). Review of Ka-Band power amplifier. *Electronics, 11(6), 942.* https://doi.org/10.3390/electronics11060942

[12] bin Wan, W. M. E. A., Ruslan, S. H., & Soh, M. J. C. (2017). Design of Low Power CMOS Bioamplifier in 250 nm and 90 nm Technology Node. *International Journal of Integrated Engineering*, *9*(4).

[13] Cimbili, B., Friesicke, C., van Raay, F., Wagner, S., Bao, M., & Quay, R. (2023). 2.6-and 4-W E-band GaN power amplifiers with a peak efficiency of 22% and 15.3%. *IEEE Microwave and Wireless Technology Letters*, 33(6), 847-850. https://doi.org/10.1109/LMWT.2023.3268522

[14] Zhang, Q., Zhao, C., Li, W., Yu, Y., Wu, Y., Liu, H., ... & Kang, K. (2023). A Ka-Band SiGe High-Gain Power Amplifier With Stability–Efficiency–Reliability-Enhanced Serial–Parallel Current-Reuse Technique. *IEEE Transactions on Microwave Theory and Techniques*, 71(3), 1657 - 1673. https://doi.org/10.1109/TMTT.2023.3308174

[15] Jobaneh, H. H. (2023). An Approach to Increase Power-Added Efficiency in a 5 GHz Class E Power Amplifier in 0.18 µm CMOS Technology. *IET Circuits, Devices & Systems*, (1), 5586912. https://doi.org/10.1049/2023/5586912

[16] Chien, J. S. C., Lee, W., & Buckwalter, J. F. (2023). High-efficiency 200-GHz neutralized common-base power amplifiers in 250-nm InP HBT. *IEEE Journal of Microwaves*, 3(2), 715-725. https://doi.org/10.1109/JMW.2023.3249203

[17] Li, D., & Du, S. (2019). A 3.5-GHz class-F power amplifier with current-reused topology in 0.13-µ m CMOS for 5G application. *Journal of Circuits, Systems and Computers, 28(11), 1950193.* https://doi.org/10.1007/s11277-022-10064-x

[18] Hasan, A. F., Murad, S. A. Z., & Bakar, F. A. (2021, May). A 3.5 GHz hybrid CMOS Class E power amplifier with reverse body bias design for 5G applications. In *AIP Conference Proceedings (Vol. 2339, No. 1). AIP Publishing.* https://doi.org/10.1063/5.0044534

[19] Du, S., Sun, Y., & Yin, H. (2023). A 3.5 GHz Class-F Power Amplifier Designs Using Current-Reused Technology for 5G Application. *Wireless Personal Communications, 128(4), 2667-2684.* https://doi.org/10.1007/s11277-022-10064-x

[20] Li, J., Wu, Y., & Lv, X. (2022, August). Study on a 0.13-µm CMOS Class-E 2.4 GHz Adjustable Power Amplifier for IoT Application. In *2022 International Conference on Microwave and Millimeter Wave Technology (ICMMT)* (pp. 1-3). IEEE. https://doi.org/10.1109/ICMMT55580.2022.10023155

[21] Seidel, A., Gündel, A., Kreißig, M., Stärke, P., Wagner, J., & Ellinger, F. (2019, October). 3.6 GHz Integrated Inverse Class-E Amplifier with Polar Modulation Capability. In 2019 *49th European Microwave Conference (EuMC)* (pp. 828-831). IEEE. https://doi.org/10.23919/EuMC.2019.8910913

[22] Zainol Murad, S. A., Hasan, A. F., & Mohyar, S. N. (2024). A 46% PAE, 2.4-GHz Two-Stage Class E Power Amplifier Utilizing CMOS 0.13-µm Technology. *IETE Journal of Research*, 1-8. https://doi.org/10.1080/03772063.2024.2368632