INTERNATIONAL JOURNAL OF INTEGRATED ENGINEERING
ISSN: 2229-838X e-ISSN: 2600-7916

IJIE

Vol. 16 No. 9 (2024) 314-325
https://publisher.uthm.edu.my/ojs/index.php/ijie

The Effects of Novel Sandwich Wafer Mounting Technique on Silicon Wafer Chipping Performance

Mohd Syahrin Amri[1,2], Ghazali Omar[1,2]*, Mohd Syafiq Mispan[3], Fuaida Harun[4], Abdul Halim Dahalan[3]

[1] *Centre for Advance Research on Energy, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, Durian Tunggal, Melaka, 76100, MALAYSIA*

[2] *Faculty of Mechanical Technology and Engineering, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, Durian Tunggal, Melaka, 76100, MALAYSIA*

[3] *Faculty of Electronics and Computer Technology and Engineering, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, Durian Tunggal, Melaka, 76100, MALAYSIA*

[4] *Infineon Technologies (M) Sdn. Bhd, Batu Berendam FTZ, 75350 Melaka, MALAYSIA*

*Corresponding Author: ghazali@utem.edu.my
DOI: https://doi.org/10.30880/ijie.2024.16.09.026

Article Info

Received: 12 May 2023
Accepted: 29 August 2024
Available online: 30 December 2024

Keywords

Backgrinding marks, chipping, dicing, novel wafer mounting

Abstract

Backgrinding marks can result in uneven mounting, which can lead to inadequate adhesion on the conventional single-sided wafer mounting process. This lack of adhesion can create instability during dicing and may result in the formation of high chipping issues. High die chipping, which may contribute to the formation of cracked dies, is a significant quality issue for semiconductor manufacturers. Due to the inability to consistently detect crack formation during testing, assessing a method that minimizes chipping during dicing the wafer is crucial. This study introduced novel double-sided mounting techniques to assess the chipping performance of the wafer dicing process on wafers with backgrinding marks. Three non-circuitry silicon wafers were evaluated with 300 µm wafer thickness and 6 x 6 mm die size including various mounting techniques were tested. The objectives of novel mounting techniques introduced in this publication, including double-sided semi sandwich and full sandwich wafer mounting techniques, added a cushioning effect and additional gripping methods for higher stability during the dicing process. The full sandwich double-sided mounting technique demonstrated significant improvement in wafer dicing chipping performance compared to the conventional single-sided mounting process with 30 die samples per wafer inspected. The results indicated that the average area of chipping, which was 0.984 mm^2 in the conventional mounting procedure, was dramatically decreased to an average of 0.0011 mm^2 with the application of the novel full sandwich mounting technique. This represents a remarkable improvement of 99.89%. The results of this study suggest that the new mounting technique can effectively minimize die chipping during wafer dicing, which can improve the quality and yield of semiconductor products.

This is an open access article under the CC BY-NC-SA 4.0 license.

1. Introduction

Wafer back grinding, mounting, and dicing are crucial process in semiconductor Integrated Circuit (IC) manufacture that have a substantial impact on the quality and reliability of the final product. One of the most significant issues that arises during the semiconductor manufacturing process is the need to minimize chipping and prevent cracking during dicing the silicon wafer which can result in yield losses, as well as a reduction in the quality and reliability performance of the device. Chipping refers to the undesirable breaking or missing of silicon wafer parts during the cutting process. According to Bryan Christian, high backside chipping potentially cause cracking in the silicon die during the mechanical dicing process due to the vibration [1] that occurred.

In this activity, the wafer back grinding process commences with the reduction of the wafer thickness from 775 µm to 300 µm through coarse and fine grinding phases with diamond grit wheels. The basic back grinding, however, results in the formation of backgrinding marks [2], which can lead to adhesion issues during wafer mounting and increase the probability of chipping during dicing. Samed Barnat's research suggests that fine and wet etch grinding can produce smoother surfaces and potentially reduce these issues. but the basic back grinding process is still extensively used due to its cost efficiency.

Wafer mounting in semiconductor manufacturing is the second process after back grinding [3]. Wafer mounting is a process of attaching a wafer to a wafer ring using mounting tape, which acts as a carrier [4] for wafer dicing operations. Several types of Ultraviolet (UV) and non-UV mounting tape are commonly used in the production floor during the wafer mounting process. UV mounting tape exhibits superior adhesion strength compared to non-UV mounting tape. This allows for secure attachment of the wafer's back, resulting in enhanced stability during dicing and reduced occurrence of chipping which similar conclusions were found by Mohd Khairul in his research [5]. However, UV mounting tape requires UV curing after the dicing process to reduce adhesive strength for the die pick-up [6] process.

Dealing with wafers that have back grinding marks can be quite challenging. The uneven surface can make it difficult for the wafer to stick to the mounting tape, leading to potential problems like slippage and instability during the dicing process. This occurs when using the traditional single-sided wafer mounting method. To tackle these challenges, a novel double-sided wafer mounting technique was developed. These techniques aim to improve the adhesion and gripping of the wafer, which also minimizes the risk of chipping.

During the last stage of the process, known as wafer dicing, a mechanical dicing saw equipped with a diamond blade is used to cut the mounted wafer into smaller pieces called "die". This stage is challenging since chipping is unavoidable [7] due to the brittle nature of the material [8],[9],[10]. High chipping can result in damage or harm to an integrated circuit's operation [11],[12],[13], which reduces the overall yield and efficiency of the manufacturing process. Vibration during dicing, high blade rotation speeds, and high-water pressure complicate the operation, especially if the wafer is not securely held. Through the brainstorming, the team believes that optimizing the double-sided mounting processes and utilizing high-quality mounting tapes makes it feasible to minimize chipping and enhance the total production yield and device performance.

2. Material and Methodology

This section contains detailed information about the materials involved, key parameters and equipment used on each process.

2.1 Backgrinding

In the backgrinding operation, the final thickness of all silicon wafers was reduced to 300 µm. The grinding parameters used were the same for each wafer. With Disco Fully Automatic Grinder/Polisher DGP 8760, the process began with mechanical Z1 rough grind (360 grit) and then followed by Z2 mechanical fine grind (2000 grit) which is the standard backgrinding and activities were done in the ST Microelectronics production floor. The basic back-grinding process already generates an initial stress [15] towards the silicon wafer [16] and to create the worst-case scenario, the decision was not to polish the wafer back. The unlevel of the wafer's back from the grinding marks makes a very huge challenge for wafer mounting process to achieve an improvement in chipping performance during the wafer dicing process. The backgrind marks pattern then were analyzed towards the chipping area to understand the correlations. It is important to assess the novel double-sided wafer mounting techniques to ensure a firm hold on the wafer in order to reduce chipping and maintain die strength [17] for silicon wafers with back grinding marks.

2.2 Wafer Mounting

The wafer mounting process is where the improvement activities were initiated for this activity. The single-sided conventional wafer mounting was set as a base since it was a standard mounting process used on the manufacturing floor. The UV mounting tape A with higher tape adhesion was used for the conventional mounting process for comparison with the novel double-sided wafer mounting techniques. For the novel double-sided

mounting approach, two techniques were introduced which called as semi sandwich and full sandwich wafer mounting. The UV mounting tape B with lower adhesion was evaluated as well to see the chipping and peeling surface overall performance.

2.2.1 Semi Sandwich Wafer Mounting Technique

The semi sandwich wafer mounting technique was developed to provide a cushioning effect and reduce vibration during wafer dicing. The purpose of the cushioning effect is to further reduce the vibration during the dicing process and improve the backside chipping performance. The semi sandwich double-sided wafer mounting technique requires a few more steps than the single-sided conventional technique, which requires laminating on the wafer surface with UV mounting tape as an initial step. Once the wafer surface succeeds laminated by the UV mounting tape, then the tape was manually cut using a manual cutter. The laminated wafer surface was then allocated on the mounting chuck table and continued to mount as normal to complete the process. The semi sandwich wafer mounting provides additional laminating on the wafer surface to absorb the vibration during the dicing process and to improve the backside chipping performance.

2.2.2 Full Sandwich Wafer Mounting Technique

The full sandwich wafer mounting technique was developed to provide extra gripping during dicing process by extending the surface laminating area. This technique was assessed to understand whether lowest chipping outcome could be achieved with additional gripping area. The full sandwich wafer mounting is a continuation of conventional mounting technique by further laminating up to the wafer ring surface area. The wafer ring and non-circuitry wafer was mounted using UV mounting tape as a first step. The second step performing a mounting process on the mounted wafer again to cover the wafer surface up to the wafer ring area. This provides extra interlocking between the UV mounting tape, the wafer surface and the wafer back area. By having this technique, the mounted wafer is expected to gain more stability during the dicing process and theoretically produce better chipping performance.

Fig. 1 shows the comparison between the conventional single-sided wafer mounting with the semi and full sandwich double-sided mounting techniques.

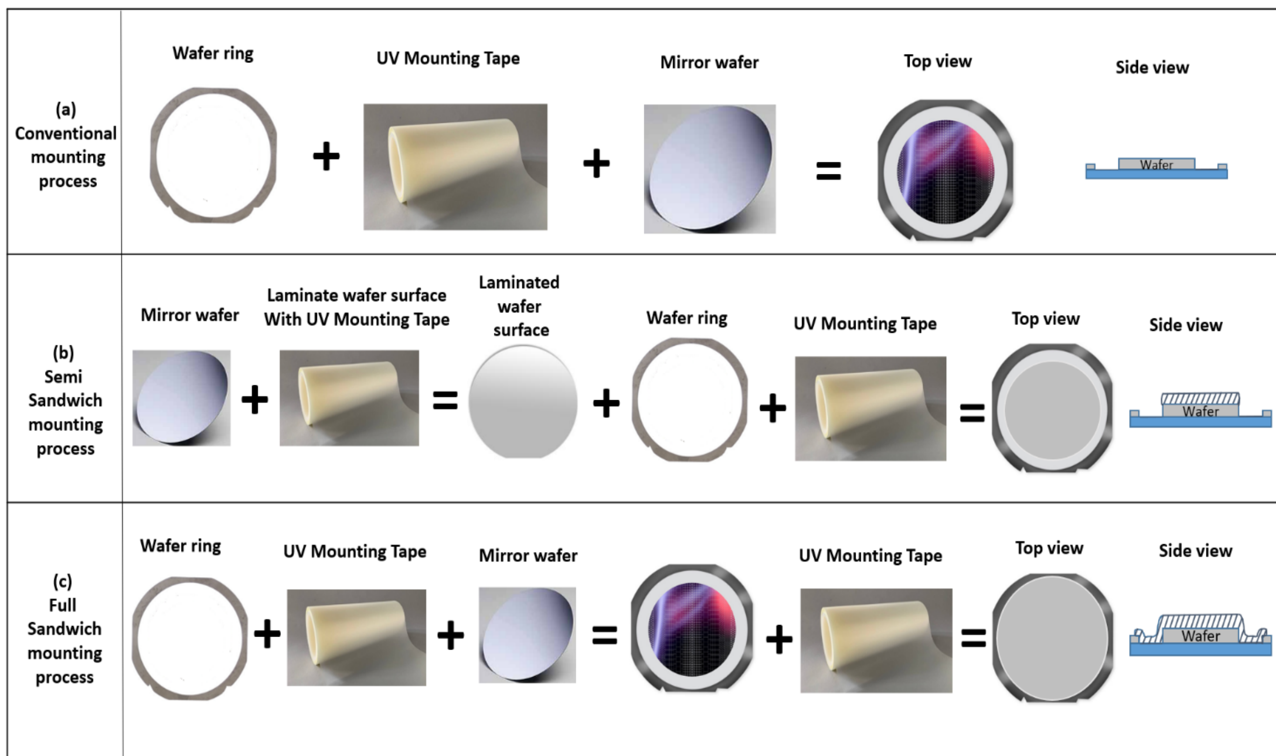

Fig. 1 *Illustration of various wafer mounting techniques (a) conventional; (b) Semi-Sandwich; (c) Full-Sandwich*

In this wafer mounting process, UV mounting tapes were used on all wafers during the evaluation on Lintec RAD-2500 wafer mounter. Before the commencement of the evaluation, the process of leveling and cleaning was carried out in order to achieve the most optimal mounting results. The mounting orientation for each mounting technique was fixed for all the wafers to reduce process variation. Table 1 presents the material setup in this

activity for the different wafer mounting techniques aimed at improving chipping and surface peeling test performance.

Table 1 *Wafer mounting technique setup*

Wafer mounting technique	Type of mounting tape on the wafer surface	Type of mounting tape at wafer back	UV curing after wafer dicing
1) Conventional mounting	No mounting tape	UV Tape A	Yes
2) Semi sandwich	UV Tape A	UV Tape A	Yes
3) Full sandwich	UV Tape A	UV Tape A	Yes
	UV Tape B	UV Tape B	Yes

In this activity, two types of UV mounting tapes were evaluated based on the surface mounting peeling test and the backside chipping performance which was inspected after the wafer dicing process. Two types of UV mounting tapes were assessed in this evaluation. The outcomes after the surface mounting peeling test and the chipping performance will be the key outcomes towards the evaluation. Table 2 defines the specifications of the UV mounting tapes that were evaluated during this activity. Both UV tapes having same overall tape thickness and the only different were the adhesion specifications before and after UV which UV Tape A having higher adhesion performance compare to UV Tape B. For this activity, those mounting technique that involve surface and wafer back such as semi and full mounting techniques will use the same type of UV mounting tape for both surface and back. The reason the full sandwich technique used UV tape A and B is because to achieve a better surface peeling performance which will be discussed further in the results and discussion section.

Table 2 *UV Mounting tape specifications*

Info		UV Tape A	UV Tape B
Tape Thickness (μm)		85	85
Base film (μm)		80	80
Adhesive layers (μm)		5	5
Adhesion	Before UV	4900	3100
(mN/25mm)	After UV	80	30

2.3 Wafer Dicing

In wafer dicing process all water parameters and dicing parameters were fixed for all the wafers and mounting techniques. Table 3 displays the dicing parameters involved during the evaluation with single-cut mode applied for all wafers.

Table 3 *Fixed wafer dicing parameter*

Parameter	Setting
Wafer thickness	0.300 mm
Die size	6.00 x 6.00 mm
Z height	0.065
Feed speed	30 mm/s
Blade RPM	40 K

The single-cut is defined as the high-precision dicing machine that uses a diamond blade to make a single pass along predefined scribe line. During the dicing process, the machine brought down the diamond blade to the cutting depth based on the parameter setting which was set to 30% of the total thickness of the UV mounting tape. The dicing machine will maintain this height for every line that the machine cuts. Once the cutting line for each line is complete the blade will raise and go down again to the same height on the next cutting line and the sequence will repeat until the whole wafer is completed cutting. Throughout the evaluation, the diamond dicing blade for

the wafer dicing process was fixed on the Disco DFD6362 Fully Automatic Dicing Saw using a blade with a blade kerf width of 22.5 ± 2.5 µm.

2.4 UV Curing

After wafer dicing, the sample wafers were delivered for UV curing using Lintec RAD-2010 curing equipment. Table 4 shares the fixed UV curing parameter used during the UV curing process on all wafers with the UV mounting tape. This was done to ensure that the UV tape on the laminated wafer surface could be peeled off and the die itself could be conveniently picked up for chipping measurement.

Table 4 *UV curing parameter setting used on all wafers*

UV Parameter	Value
Voltage	351 V
Power	1390 W
Light intensity	126 mW/cm^2
Exposure dose	552 ml/cm^2
Temperature	44.8°C
UV irradiation speed	15 mm/sec
Nitrogen purge time	7.0 s

2.5 Surface Mounting Tape Peeling Test

The peeling test performance is the initial test that should be passed to qualify for the novel wafer mounting technique. After UV curing, the diced wafers were transported for the surface mounting peeling testing procedure. The surface mounting peeling test procedure involved a cellophane tape of 60 mm (width) x 48 mm (length) during the operation. The surface mounting peeling operation must be conducted on the dicing saw chuck table with the vacuum suction activated so that the wafer is held securely and further chipping is not caused by the movement of the dies during the peeling process. The cellophane tape was then applied to the wafer surface and the peeling procedure was carried out as per Fig. 2.

Fig. 2 *Surface mounting peeling process on dicing chuck table*

Equation (1) shows how the surface peeling yield calculation was done where P is the peeling test yield, X is the total number of die per wafer and finally Y is the number of the unpeel surface mounting tape found on the wafer surface. In order to successfully pass the surface peeling test, it is necessary to attain a yield of 100%.

$$P = \frac{(X - Y)}{X} x\ 100\% \quad (1)$$

The morphological study encompassed in these activities entailed the utilization of various equipment to analyse chipping occurrences at the back of the silicon wafers. The following types of equipment were utilized throughout the evaluation process.

2.6 High Power Scope

In this activity, Zeiss Axioscope 2 MAT optical microscope was used. The scope was calibrated first before the measurement activities started. For chipping area measurements, the scope setting was based on 50x magnification. Higher magnification was then selected to check the condition for further cracking verification from the chipping area. For each wafer on every mounting technique, 30 dies were picked according to the mapping for consistent die selection in the backside chipping measurement regions. The dies were picked up using plastic tweezers and a vacuum pen to prevent chipping caused by handling. However, before the pick-up operation, the die will be inspected under 50x magnification. Higher magnification was used to inspect the chipping area that was suspected for cracking issue. Since high power scope was used to inspect on each die, the die size is too large to capture the entire inspection area under the lowest magnification (50x). The die area then divided into 12 sections for total chipping area calculation. The image for each portion will be saved according to section and then transferred to the "ImageJ" software for measuring the chipping area. Before measurement activities start, the dimensions in "ImageJ" software will be calibrated.

The chipping area will be captured in sections and then uploaded to "ImageJ" software, where the area will be measured in μm² and then converted to mm² to determine the overall chipping area. The section chipping area then will be summed up to represent the overall chipping area per die unit (6 x 6 mm = 36 mm²) and this process will be repeated up to 30 die samples per each wafer mounting technique. Recent research by Shang Gao has found the same method of calculating the chipping edge measurement using the area calculation method using AutoCAD software [18]. The only variation between the two methods was the software used to measure the chipping area, which was AutoCAD by Shang Gao and ImageJ by the author however, the chipping area measuring methods were identical. Fig. 3. Illustrate the overall methodology for chipping measurement.

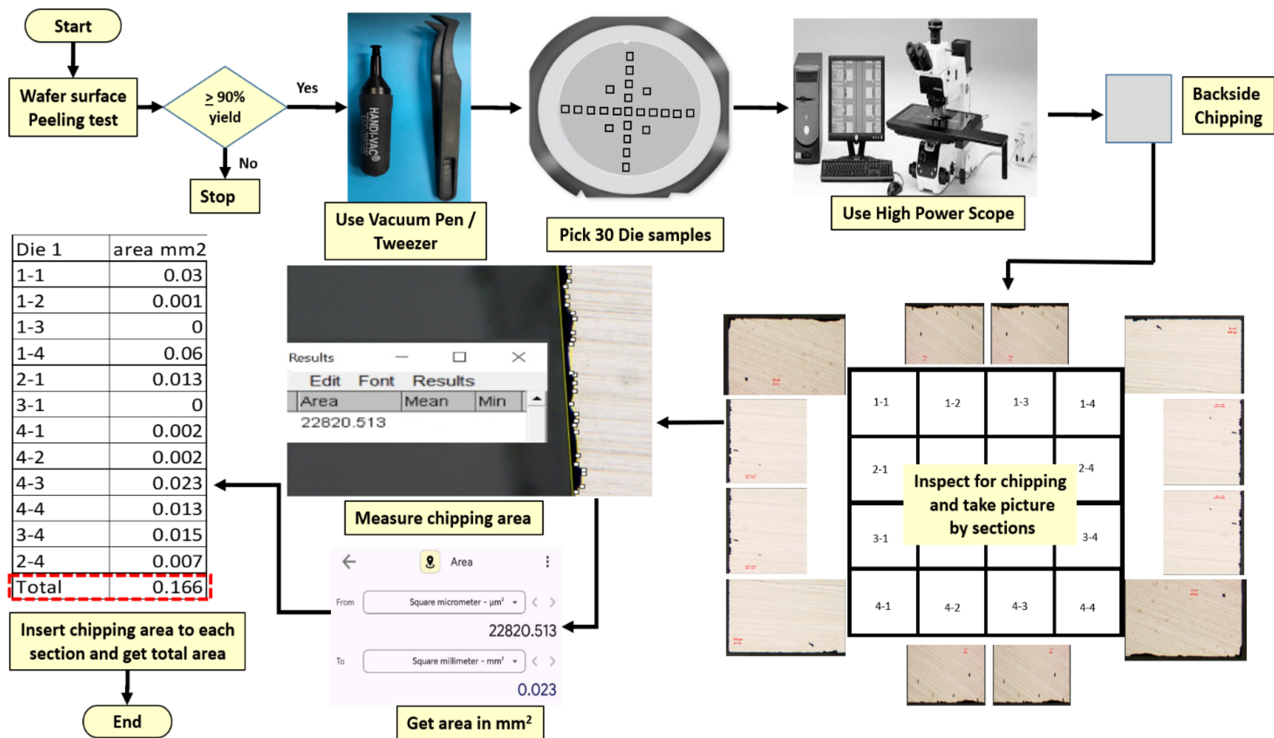

Fig. 3 *Methodology for chipping measurement*

2.7 Scanning Electron Microscope (SEM)

SEM was used to check the presence of cracks initiated from the chipping during the wafer dicing process. Inspection based on sampling die for each mounting technique was taken and inspected using SEM at every corner to ensure the samples are free from any cracking issue up to 1000 x magnification. The high magnification helps to analyse the chipping performance on each wafer mounting technique and the chipping trends as well.

2.8 3D Profilometer

A 3D profilometer is a type of instrument used to measure the surface topography of an object in three dimensions. A non-contact Shodensha GR3400 profilometer was used in this activity. It was using light to measure the surface without making any physical contact. In order to determine the factors that contribute to excessive chipping during the wafer dicing process, the topography of the wafer's backside was analyzed using a 3D profilometer. The backgrinding marks were analyzed using 3D profilometer to understand the roughness level towards the chipping performance as well.

3. Results and Discussions

In developing the novel semi and full sandwich wafer mounting techniques, the surface mounting peeling results is crucial. Table 5 provides the overall results of surface mounting peeling results on two types of UV mounting tapes. Since the standard mounting approach does not involve the application of UV mounting tape on the surface, there is no yield calculation for the conventional mounting tape technique. The semi sandwich mounting technique demonstrated better results, with a 90% yield of overall surface mounting tape successfully peeled off using UV mounting tape A. Unfortunately, UV mounting tape A does not provide consistent surface mounting peeling performance when using the full sandwich mounting technique which only achieves a 70% yield of surface peeling performance. The inconsistent peeling result on the full sandwich mounting technique was observed due to higher adhesion after UV curing performance specification. The specification showed UV mounting tape A has higher adhesion before UV curing (4900 mN/mm) and as well after UV curing (80 mN/25mm) and the decision to evaluate UV mounting tape B with lower adhesion before (3100 mN/mm) and after UV curing (30 mN/25mm) showed an excellent yield result with 100% surface mounting peeling results.

Table 5 *Surface mounting peeling results*

Wafer mounting technique	Mounting tape on wafer surface	Surface mounting peeling Yield
1) Conventional mounting	No mounting tape	Not applicable
2) Semi sandwich	UV Tape A	90%
3) Full sandwich	UV Tape A	70%
	UV Tape B	100%

Xing Wu reported that the adhesive in UV mounting tape shrinks significantly in volume after UV irradiation due to the polymerization of multifunctional oligomers, resulting in a significant decrease in peel strength [19] and a lower value after UV curing on UV tape B produced lower peel strength resulting for better surface peeling results. The UV tape B specification has lower adhesion before curing, thus additional testing is needed to determine how well it grips the wafer during dicing, which could affect chipping on the backside. The samples were then sent for chipping inspection using a high-power scope to ensure the overall performance of the chipping area. The backside chipping performance of each sample was examined at a magnification of 50x. To ensure that the chipping area was free of cracks, a higher magnification was utilized towards the chipping area. No visible signs of cracks were detected during the visual inspections of all finished samples. Additional investigation into the behavior of backside chipping and cracks on die samples was conducted using scanning electron microscopy (SEM). As illustrated in Fig. 4, no evidence of crack propagation was also found using the wafer mounting procedures at magnifications of 100, 400, or 1000 and the images showed that full sandwich wafer mounting techniques provide the lowest backside chipping performance.

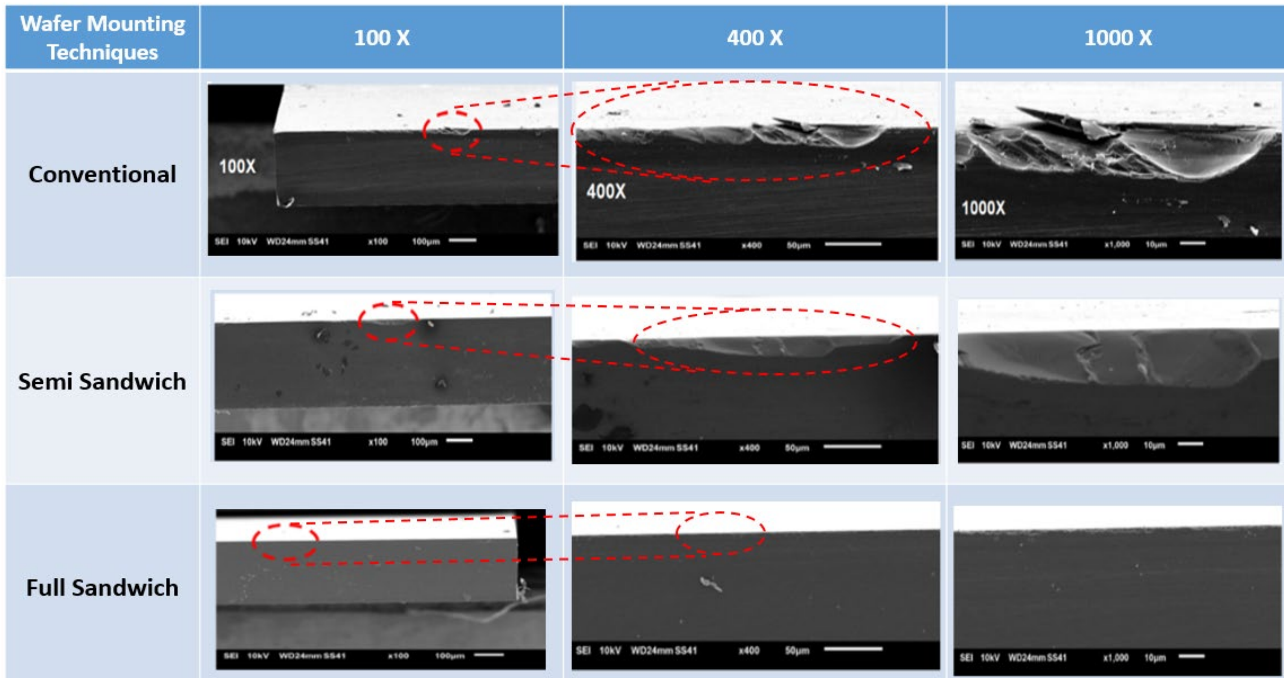

Fig. 4 *Backside chipping monitoring using SEM on all mounting techniques*

In order to validate the backside chipping performance, additional verification was carried out using the Analysis of Variance (ANOVA) method. This analysis was conducted on 30 samples from each mounting procedure. Results in Fig. 5 showed that the full sandwich wafer mounting technique had significantly the lowest backside chipping performance, while semi sandwich wafer mounting had a second lower backside chipping performance compared to the conventional wafer mounting technique. The performance is significantly different by looking at the isolated ring on the graph's right side. The utilization of novel semi and full sandwich wafer mounting techniques, involving the application of mounting tape on the wafer surface, resulted in a cushioning effect and ensured secure stability of the wafer during the cutting process. This has led to a decrease in the backside chipping performance, in comparison to the conventional mounting technique that does not involve the use of UV mounting tape on the wafer surface. The extended UV mounting tape on the wafer surface in the full sandwich wafer mounting approach exhibited superior adhesion to the wafer throughout the dicing process, resulting in the lowest occurrence of chipping on the backside. The conventional mounting approach, which does not involve using mounting tape on the wafer surface, lacks support during the dicing process, leading to significant vibration and the highest level of backside chipping.

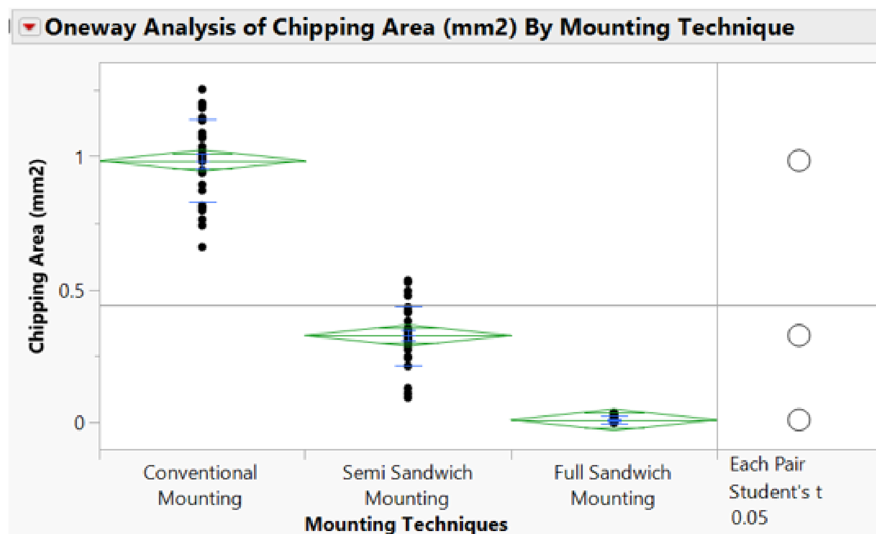

Fig. 5 *ANOVA results on silicon wafer backside chipping performance*

Observation showed two types of grinding marks at the wafer backside near the chipping area. The first type is the chipping parallel with grinding marks and the second type is chipping perpendicular with grinding marks. The chipping areas toward the grinding mark were then further studied using a 3D profilometer to determine the surface roughness difference between parallel and perpendicular chipping behavior toward the grinding mark. This is to determine whether there is a correlation between the chipping and the grinding mark. The arithmetical mean roughness value (Ra) and mean roughness depth (Rz) were monitored to understand the behavior between two chippings toward the grinding marks. Ra is the average of surface roughness while Rz is the height between the surface's highest "peak" and lowest "valley". The surface roughness of the high chipping area was examined by considering both parallel and perpendicular directions to the grinding mark, and then compared accordingly. The wafer back exhibited two distinct chipping conditions: conventional low chipping and high chipping areas. Surface roughness measurements were conducted to gather information about the surface.

Table 6 contains the compilation of surface roughness on a few samples. In addition, it was discovered that Hao Nan Li used Ra and Rz for surface measurement monitoring [20], which demonstrates that the process is fairly comparable. The results presented in Table 5 indicate that the parallel chipping value exhibited higher mean roughness values (Ra) and mean roughness depths (Rz) compared to the perpendicular chipping approaching the grinding mark.

Table 6 *Surface roughness comparison of high and low chipping toward parallel and perpendicular grinding marks*

Parallel (Ra)	
High Chipping area	3.1 µm
Low Chipping area	4.1 µm

Perpendicular (Ra)	
High Chipping area	0.8 µm
Low Chipping area	0.9 µm

Parallel (Rz)	
High Chipping area	23.5 µm
Low Chipping area	17.1 µm

Perpendicular (Rz)	
High Chipping area	5.2 µm
Low Chipping area	5.1 µm

To verify whether the parallel and perpendicular have significant impact on the grinding marks, a statistical test was conducted. A T-test is a statistical test employed to ascertain the presence of a substantial disparity between the means of two groups. It is frequently employed in hypothesis testing to compare the means of two samples or to compare a sample mean to a known value. In the context of a T-test, the p-value is a statistical parameter that aids in determining the significance of the results. The T-test was used to verify the significance of the test based on 30 sample units. The purpose of this test is to determine whether the parallel or perpendicular has chipping effects toward the grind mark pattern. The T-test was based on a significance level (α) of 0.05. Fig. 6 illustrates the T-test findings comparing the location of chipping and grinding markings (parallel or perpendicular). The results indicate there is no significant difference in positioning between the chipping and grinding marks, as indicated by the combined ring on the right-hand side of the graph. Based on the results, we can infer that there is no significant difference in the grinding marks' orientation (parallel or perpendicular) with respect to the chipping performance. Therefore, according to the T-Test results, the grinding marks pattern has no impact on the chipping performance at any of the places. Shang Gao [18] also reported comparable findings, indicating that there were no significant differences in crystal orientation and chipping edge size at different locations.

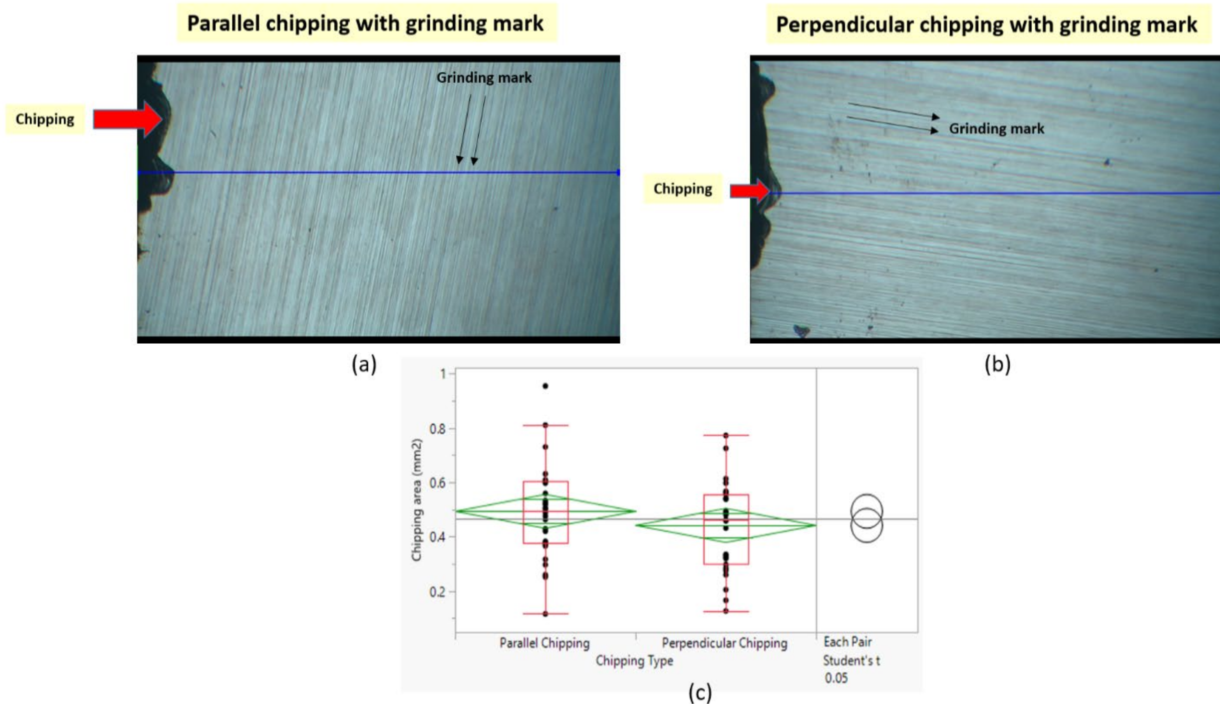

Fig. 6 *(a) Parallel chipping; (b) Perpendicular chipping; (c) T-Test results comparing chipping towards grinding mark patterns*

4. Conclusions and Future Work

Based on the analytical findings, it is possible to draw several conclusions regarding the activities:

1) Applying the lowest adhesion of UV mounting tape towards the novel double-sided wafer mounting techniques provides excellent surface peeling tape yield without affecting the backside chipping and crack performance.
2) The full sandwich wafer mounting technique provides additional gripping and the highest interlocking area on the wafer surface up to the wafer backside area resulting in the lowest backside chipping performance
3) The backgrinding marks pattern produced by the wafer back grinding process does not influence the chipping performance during the wafer dicing process

Since the evaluation uses the non-circuitry wafers, the author suggested that future testing be conducted on circuitry wafers for better understanding of the overall performance. However, the novel full sandwich mounting techniques have given some ideas on how to improve the wafer mounting process for higher cutting stability during the wafer dicing process by implementing the double-sided mounting technique.

Acknowledgement

The author would like to thanks Universiti Teknikal Malaysia Melaka (UTeM), Mr. Chow Peng Fei from Lintec Advanced Technologies (M) Sdn Bhd, Ms. Vling Loo from Disco Hi-Tec (Malaysia) Sdn Bhd and Mr. Azman bin Teh from STMicroelectronics Muar Sdn Bhd for supporting and contributing towards this paper.

Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

Author Contribution

The authors confirm their contribution to the paper as follows: ***study conception and design:*** *Mohd Syahrin Amri, Ghazali Omar, Mohd Syafiq Mispan, Fuaida Harun;* ***data collection:*** *Mohd Syahrin Amri;* ***analysis and interpretation of results:*** *Mohd Syahrin Amri Ghazali Omar, Mohd Syafiq Mispan, Fuaida Harun, Halim Dahalan* ***draft manuscript preparation:*** *Mohd Syahrin Amri Ghazali Omar, Mohd Syafiq Mispan. All authors reviewed the results and approved the final version of the manuscript.*

References

[1] B. C. S. Bacquian (2020) Dicing before Grinding : A Robust Wafer Thinning and Dicing Technology, vol. 11, no. 4, pp. 25–34, https://doi.org/10.9734/JERR/2020/v11i417067.

[2] S. Barnat, H. Frémont, A. Gracia, and E. Cadalen, (2012) Evaluation by three-point-bend and ball-on-ring tests of thinning process on silicon die strength, *Microelectron. Reliab.*, vol. 52, no. 9–10, pp. 2278–2282, https://doi.org/10.1016/j.microrel.2012.06.093.

[3] K. Aizawa, Jun Maeda, Y. Hasegawa, and Shinya Takyu, (2018) A Study on Back Grinding Tape for Ultra-thin Chip Fabrication, pp. 86–89,.

[4] K. J. Kim (2013) Development of waxless wafer mounting system for silicon wafer polishing process, *Appl. Mech. Mater.*, vol. 339, pp. 762–765, https://doi.org/10.4028/www.scientific.net/AMM.339.762.

[5] M. K. Bin Zainal, A. Bin Abdul Aziz, and V. Ramalingam (2022) Backside Chipping Investigation & Improvement on TiNiVAg Back Metal Silicon Die, *Proc. IEEE/CPMT Int. Electron. Manuf. Technol. Symp.*, vol. -Octob, pp. 0–3, 2022, https://doi.org/10.1109/IEMT55343.2022.9969494.

[6] B. Sun *et al.* (2022) Fully cross-linked UV-induced peelable acrylic PSA prepared from a dual curable castor oil based urethane acrylate oligomer for wafer dicing, *Prog. Org. Coatings*, vol. 163, no. December, p. 106680, https://doi.org/10.1016/j.porgcoat.2021.106680.

[7] C. S. Premachandran *et al.* (2015) Wafer level high temperature reliability study by backside probing f or a 50um thin TSV wafer, *Proc. - Electron. Components Technol. Conf.*, vol. 2015-July, pp. 2144–2148, https://doi.org/10.1109/ECTC.2015.7159899.

[8] D. Xue, C. Zhong, E. Zhang, W. Jiang, and C. Zhang, (2021) Die chipping FDC development at wafer saw process, *2021 22nd Int. Conf. Electron. Packag. Technol. ICEPT 2021*, https://doi.org/10.1109/ICEPT52650.2021.9568039.

[9] J. Shen, X. Zhu, J. Chen, P. Tao, and X. Wu, (2019) Investigation on the edge chipping in ultrasonic assisted sawing of monocrystalline silicon, *Micromachines*, vol. 10, no. 9, https://doi.org/10.3390/mi10090616.

[10] F. Inoue *et al.*, (2020) Morphological characterization and mechanical behavior by dicing and thinning on direct bonded Si wafer, *J. Manuf. Process.*, vol. 58, no. January, pp. 811–818, https://doi.org/10.1016/j.jmapro.2020.08.050.

[11] F. Inoue *et al.*, (2017) Influence of Si wafer thinning processes on (sub)surface defects, *Appl. Surf. Sci.*, vol. 404, pp. 82–87, https://doi.org/10.1016/j.apsusc.2017.01.259.

[12] T. J. Su, Y. F. Chen, J. C. Cheng, and C. L. Chiu, (2018) An artificial neural network approach for wafer dicing saw quality prediction, *Microelectronics Reliability*, vol. 91. pp. 257–261,. https://doi.org/10.1016/j.microrel.2018.10.013.

[13] S. Takyu *et al.*, (2016) A Novel Dicing Technologies for WLCSP Using Stealth Dicing through Dicing Tape and Back Side Protection-Film, *Proc. - Electron. Components Technol. Conf.*, vol. 2016-Augus, pp. 1241–1246, https://doi.org/10.1109/ECTC.2016.138.

[14] Y. M. Hsieh, R. Lu, J. W. Lu, F. T. Cheng, and M. Adnan, (2020) Automated classification scheme plus AVM for wafer sawing processes, *IEEE Robot. Autom. Lett.*, vol. 5, no. 3, pp. 4525–4532, https://doi.org/10.1109/LRA.2020.3000678.

[15] H. Ling, C. Yang, S. Feng, and H. Lu, (2020) Predictive model of grinding residual stress for linear guideway considering straightening history, *Int. J. Mech. Sci.*, vol. 176, Jun., https://doi.org/10.1016/j.ijmecsci.2020.105536.

[16] H. Liu, T. Yang, X. Tian, S. Chen, F. Dong, and J. Han, (2022) Iterative method for obtaining nonuniform grinding-induced residual stress distribution of silicon wafers based on global deformation, *Mater. Sci. Semicond. Process.*, vol. 150, no. July, p. 106971, https://doi.org/10.1016/j.mssp.2022.106971.

[17] H. Sekhar, T. Fukuda, K. Tanahashi, and H. Takato, (2019) "The impact of silicon brick polishing on thin (120 μm) silicon wafer sawing yields and fracture strengths in diamond-wire sawing," *Mater. Sci. Semicond. Process.*, vol. 105, no. September 2019, p. 104751, https://doi.org/10.1016/j.mssp.2019.104751.

[18] S. Gao, R. Kang, Z. Dong, and B. Zhang, (2013) Edge chipping of silicon wafers in diamond grinding, *International Journal of Machine Tools and Manufacture*, vol. 64. pp. 31–37,. https://doi.org/10.1016/j.ijmachtools.2012.08.002.

[19] X. Wu, F. Ren, H. Ma, Z. Zhou, and W. Xu, (2022) The effect of surface morphology on the peel performance of UV-induced adhesion-reducing adhesives, *Mater. Res. Express*, vol. 9, no. 2, doi: 10.1088/2053-1591/ac4e40.
[20] H. N. Li, T. B. Yu, L. Da Zhu, and W. S. Wang, (2017) Analytical modeling of ground surface topography in monocrystalline silicon grinding considering the ductile-regime effect, *Arch. Civ. Mech. Eng.*, vol. 17, no. 4, pp. 880–893, https://doi.org/10.1016/j.acme.2017.03.010.