A Novel Hybrid Full Adder using 13 Transistors

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Abstract: Full adder is a basic and vital building block for various arithmetic circuits such as multipliers. In this paper, a hybrid 1-bit full adder using complementary metal-oxide semiconductor (CMOS) logic style had been designed. This hybrid adder divided into three modules. Module I is a three transistors XOR gate. Module II is a novel sum circuit which successfully modified with the usage of lesser number of transistors used. Module III is a carry circuit which uses the carry output of module I and several other input to generate carry output. Performance parameters such as power and delay were compared to some of the existing designs. With a 1.8V voltage supply, the average power consumption of proposed hybrid adder was found extremely low which is 2.09 µW and a very low delay of 350 ps. Design in both speed and energy consumption becomes even more significant as the word length of the adder increases. The full adder design is simulated using Tanner EDA version 16 using General Process Design Kit (GPDK) 250nm technology CMOS processes.

Keywords: Adder, Hybrid design, Sum circuit, Low power

1. Introduction

Due to continuous scaling of MOS devices, the number of transistors on single chip increases tremendously and also operating frequency increases with technology. For this reason, design of low power, high speed adder has become most vital. Full adders had known as the most fundamental building block of most of the circuit application, such as notebooks, cellular phone. This remains a key domain focus of the researchers throughout the years [1]. Several logic styles have been used in the past to design full adder cells and each design has its own advantages and disadvantages.

In the recent year, many new circuits are proposed using less number of transistors with less delay and low power requirement but different logic tend to prefer certain performance aspect. The standard complimentary style-based adders which made up of 28 transistors has the advantages of robustness against voltage scaling and regular layout [2, 3] but it required high input capacitance [1]. Another smart design is the hybrid CMOS full adder which used up 20 transistors. This full adder has good characteristic in term of speed and power; while the demerits of this design relay on the modified semi XOR-XNOR gates which not able to generate full swing for all output [4]. Later, another 16 transistors hybrid adder had been proposed by Partha [1]. This design was compared with other existing full adder designs and was found to offer significant improvement in terms of power and speed but the main concern of this design was consumed slightly larger area than some others design. Similarly, another 16 transistors full adder which used XOR and AND gate had been proposed [5]. This design able to achieve the low power and high speed by removing the inverter and balance its delay generating but the greatest drawback of this design is it produced incomplete voltage swing. It can be figured out that researchers nowadays tend to focus on the hybrid logic approach which included various logic styles in order to improve the overall performance of the full adder.

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2. Proposed Full Adder

The proposed full adder circuit is designed by breaking the full adder in to three modules as shown in *Figure 1*. Module I is an XOR-XNOR circuit which drives the other modules, module II generate the sum signal (SUM) modules III generates carry signals (C_{OUT}). Both of these module relay on the output of the first module, thus module I must have good driving capability and able to produce full swing outputs simultaneously. Each modules is designed individually so that it able to be optimized in terms of power, delay and area. The details of modules are discussed next.

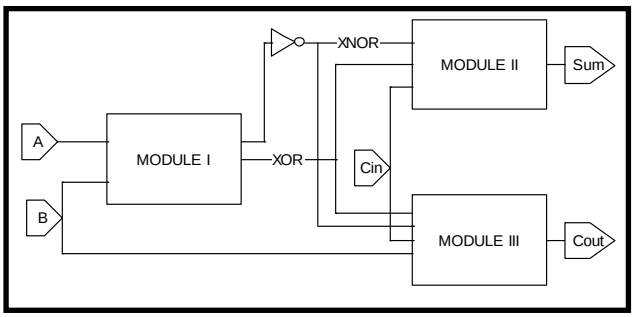

Figure 1 Block Diagram for Hybrid Full Adder

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A. 3T XOR Module

Module I made up of three transistor (3T) XOR gate as shown in *Figure 2*. The design is based on a modified version of CMOS inverter and a PMOS pass transistor [6].

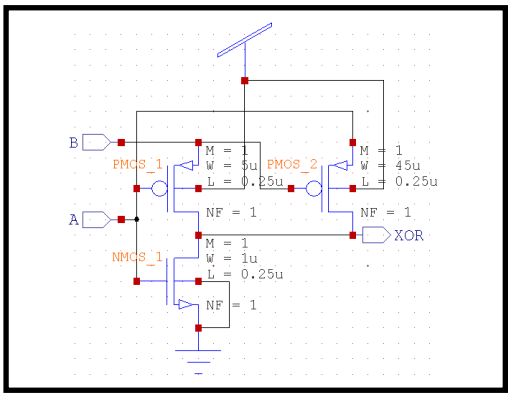

Figure 2 Module I 3T XOR Circuit

When input B is logic high which is '1', the inverter work as CMOS inverter. While input logic is at logic low which is '0', the CMOS inverter output is at high impedance. However, the pass transistor PMOS_2 is enabled and the output produced will be same as input A [7]. The operation at this time functions as a two input XOR gate. Thus it can be concluded that output OUT is the complement of input A. Nevertheless, voltage degradation happened when A=1 and B=0, due to threshold voltage drop across transistor PMOS_2. This problem can be minimized by adjusting the W/L of transistor in order to achieve full swing output.

B. Modified SUM Module

Module II is designed by modifying the Sum Circuit used in the previous research that proposed by A.Suguna [8]. Six transistors were used in the previous research to make this circuit worked. In this paper, a new design had been proposed as shown in *Figure 3* which only use four transistors for sum circuit.

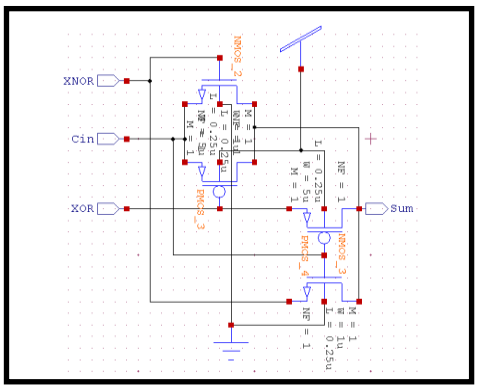

Figure 3 Module II Sum Circuit

When XOR gate is provided with logic '0', XNOR gate will be provided with logic '1'. Both XOR and XNOR are used to control the gate for the transmission gate while the input is provided by C_{IN}. While the gates for PMOS and NMOS below are controlled by input of C_{IN}. Either logic '0' or logic '1' is passed depends on output of XOR and XNOR gate. Logic high passes by NMOS while logic low passes by PMOS. Inverter is reduced in this new design to reduce power consumption and area used.

C. Carry Generation Module

Module III made up of two set of transmission gate which controlled by XNOR and XOR gate respectively. The output carry signal is implemented by two PMOS and two NMOS as shown in *Figure 4*. The input carry signal (C_{IN} / B) only propagates through only one transmission gate, this able to minimize the overall carry propagation path. The deliberate use of strong transmission gate able to further reduce the propagation delay effectively.

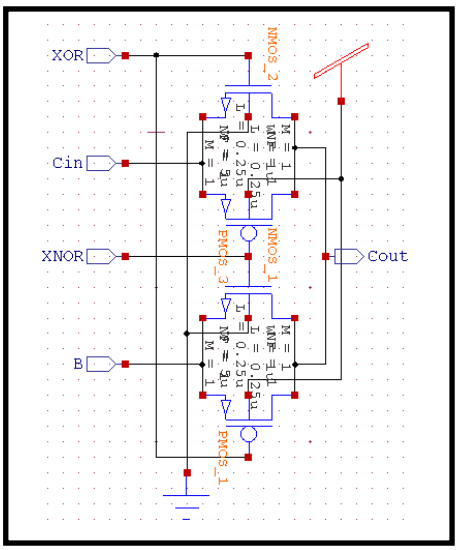

Figure 4 Module III C_{OUT} Circuit

3. Results and Discussion

The analyses of the circuits were performed on Tanner EDA version 16 GPDK 250nm CMOS process. The schematic of the proposed hybrid full adder is drawn using S-edit and the tested output waveform are shown in *Figure 5* and *Figure 6*. The design is furthered on to layout design using L-edit and is shown in *Figure 7*.

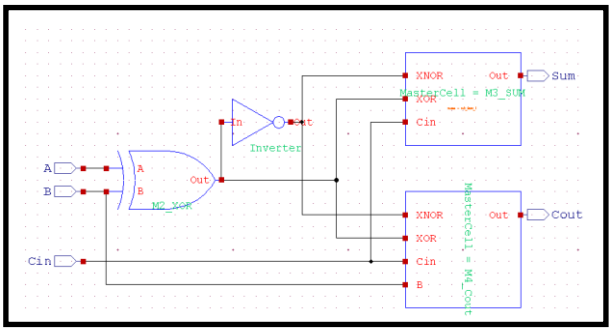

Figure 5 Schematic Diagram for Hybrid Full Adder Circuit

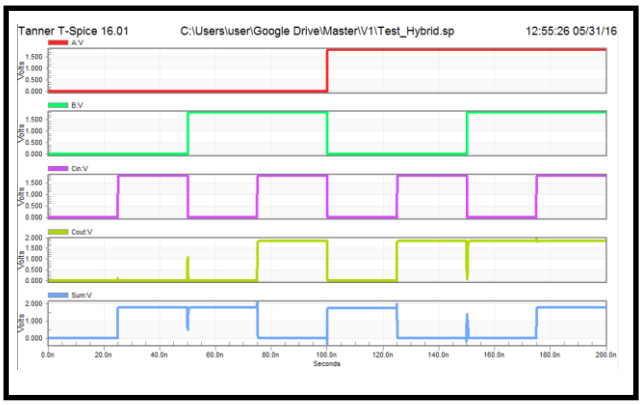

Figure 6 Output Waveform for Hybrid Full Adder Circuit

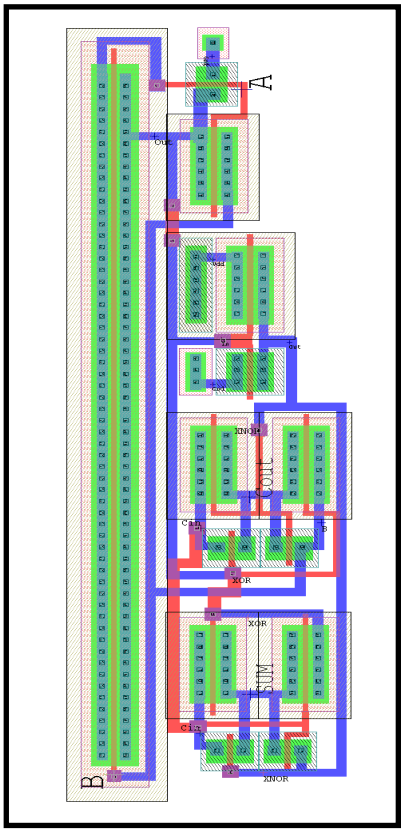

Figure 7 Layout for Hybrid Full Adder Circuit

A. Comparison of Delay for Full Adders

Comparison of the delay at the supply voltage range of 1-1.8V of reported and proposed circuit is shown in Table 1. This comparison table is arranged from the highest number to the lowest number of transistors used in a full adder. The proposed full adder used a bigger GPDK as compared to others but it still able to give a comparable performance with other full adders.

Table 1 Comparison of Delay in Different Full Adder

	Power supply (V)	Transistor (T)	Delay (ps)	Technology
[3]	1	28	243	Tanner EDA-32nm CMOS Technology
[4]	1	20 (GDI + MUX)	1120	SPICE-90nm CMOS Technology
[4]	1	20 (Hybrid)	1116	SPICE-90nm CMOS Technology
[1]	1.8	16 (Hybrid)	224	Cadence- 180nm CMOS Technology
Proposed	1.8	13	350	Tanner EDA-250nm CMOS Technology
[9]	1.2	8	185900	HISPICE-180nm CMOS technology
[9]	1.2	6	200124	HISPICE-180nm CMOS technology

By comparing the proposed full adder with the 28 transistors full adder [3] that used 32nm GPDK that have robustness against voltage scaling and transistor sizing, the proposed full adder perform a higher delay than it. Nevertheless, the 28 transistors full adder required buffer during operation thus created high capacitance and bigger area compared to the proposed full adder. For 20 transistors (Hybrid) full adder [4], the proposed full adder able to perform 68.63% than it. The full adder design required semi XOR-XNOR gate which causes it lack of ability to generate all possible output. Meanwhile, by comparing the proposed full adder with 13 transistors to 20 transistors full adder (GDI+MUX) [4], the proposed circuit able to perform 68.75% faster. For hybrid full adder that using 16 transistors with GPDK 180nm able to produce an output with a lower delay compare to the proposed full adder. The bottleneck of this full adder is it has a poor driving capability thus the output waveform will degrade when cascading happen [1]. Degradation in waveform will affect the accuracy of the result for the overall design. 8 transistors full adder and 6 transistors full adder are

being designed and its application using deep submicron technology [9]. These full adders acquire with least area among all the full adder design but it required a high delay due to the usage of transmission gate. Besides, 6 transistors full adder not able to produce output with full swing waveform [10] . This will affect the result of the final output when cascading happen. Subsequently the time delay of proposed circuit is 30%-36% higher than some of the others circuit but the proposed circuit able to provide an output with an acceptable delay range with a lower area full adder.

B. Comparison of Power Consumption for Full Adders

Comparison of the power consumed by one bit full adder at the supply voltage range of 1V-1.8V of reported and proposed circuit is shown in Table 2. Results of average power consumption of proposed full adder obtained is shown in *Figure 8.*

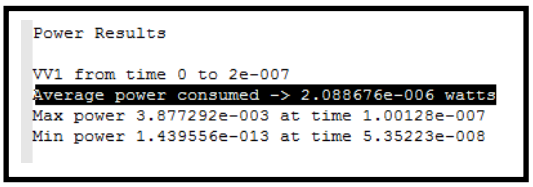

Figure 8 Power Result

Table 3 Comparison of Power Consumption in Different Full Adder

	Power supply (V)	Transistor (T)	Power Consumption (µW)	Technology
[3]	1	28	4.56	Tanner EDA-32nm CMOS Technology
[4]	1	20 (GDI + MUX)	4.36	SPICE- 90nm CMOS Technology
[4]	1	20 (Hybrid)	8.45	SPICE- 90nm CMOS Technology
[1]	1.8	16 (Hybrid)	4.16	Cadence Virtuoso-180nm CMOS Technology
Proposed	1.8	13	2.09	Tanner EDA-250nm CMOS Technology
[11]	1.8	8	116.5	Cadence Virtuoso-180nm CMOS Technology
[10]	5	6	2.29	Tanner EDA-180nm CMOS Technology

By comparing the average power consumption of the proposed full adder with the other adders which reported from [1]-[3] for the supply voltage range from 1-1.8V, the proposed full adder consumed 49.76% to 75.27% less. It can be seen that the proposed adder uses only 13 transistors whereas the other adders [3], [4], [1] require more than 16 transistors. In another design, 8 transistors are used to design a full adder but reported shows that it consumed 98.2% power than the proposed full adder. The 8 transistors adder had successfully reduced the number of transistors use to design a full adder but it also known as an impractical design [11] because it has a very large amount of power consumption. Other than 8 transistors adder, the proposed full adder also able to consume slightly lesser power than the 6 transistors adder. Nevertheless the 6 transistors adder not able to produce output with full swing waveform [10] and this will affect the final output waveform.

Conclusion

In this paper, a novel low-power 1 bit full adder cell has been proposed. A new design of Sum Circuit is produced by using only 4 transistors with the concept of pass transistors logic. The adder can be categorized under hybrid-CMOS full adder as this adder uses 3 transistors XOR gate, transmission gates and pass transistor. The performances of this circuit have been compared with other adders, the simulation results established the proposed adder offered least power consumption (2.09 µW at 1.8V) among all the reported design. It also has the merits of small delay, output with full swing waveform, and area saving due to lower transistors counts and special structures. The proposed full adder will be further used for 8-bit full adder cascading process and implement in 8x8 bit multiplier using Vedic Mathematics method. Smaller GPDK will be used in future in order to achieve better performance in term of speed, power consumption and area.

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