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49-Level Cross Switched Cascade Multilevel Inverter Fed Induction Motor Drive

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Abstract

To convert DC supply which is output of renewable energy sources to AC supply multilevel inverters are required. Multilevel inverters offer eminent solutions to high voltage high power applications due to the association of several devices in a series configuration. Multilevel inverter output voltage contains lower harmonics compared with conventional 2-level inverter. This paper presents three phase 49-level asymmetrical cross switched cascade multilevel inverter fed Induction motor drive. This topology requires less number of switches compare to cascaded H bridge. Analysis of 49-level cascade cross switched multilevel inverter fed induction motor drive is simulated on MATLAB/SIMULINK platform.

1. Introduction

Microgrids, which combine a variety of energy sources such as diesel generators, solar panels, wind turbines, fuel cells, and others to integrate with the power grid or offer capacity to local demands, are on the rise. More powerful electronic converters play an important role. Staggered inverters are more efficient at delivering force than two-level inverters, which are incapable of supplying capacity to medium- and high-power loads. The primary premise of a multi-level inverter is to distribute the inverter's working voltage between connected switches in the circuit. As a result, applications requiring high voltage/power ratings can use low appraising switches, lowering inverter costs. As level of yield voltage expands level of music diminishes at low ex-changing frequencies so cost of channels lessens [1-2].

The common issue in the aforementioned locations is that the number of switches required increases in tandem with the increase in yield voltage, which in turn increases the cost, size, and complexity of swapping and executing equipment circuits [6-8]. A balanced staggered inverter has similar upsides of DC sources, whereas an incorrect staggered inverter has inconsistent upsides of DC sources; the number of force electronic parts required for an even staggered inverter is greater than for an unbalanced staggered inverter [9-11]. This study [12-14] presents an asymmetrical 49-level cross-switched cascade multilevel inverter. Every essential unit comprises of eight changes out of eight switches six are unidirectional; two are bidirectional and two inconsistent DC sources [15-17]. Recreation of three stage 49-level for the proposed geography has been acted in MATLAB climate and results are talked about.

2. Proposed Cross Switched Cascade Multilevel Inverter

The three-phase cross switched cascaded multilevel inverter (CSCMLI) [18] is an asymmetrical multilevel inverter addressed in this paper. Eight switches make up the basic unit, six of which are unidirectional (S^1_1, S^1_2, S^1_5, S^1_6, S^1_7, S^1_8) and two of which are bidirectional (V^1_1 and V^1_2) (S^1_3 and S^1_4). In contrast to unidirectional switches, which conduct current in both directions but block voltage in just one, bidirectional switches block voltage and conduct current in both directions.

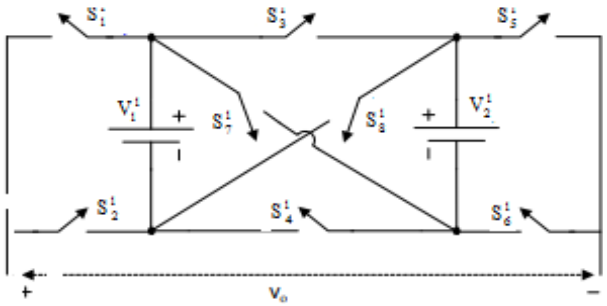

Fig. 1 *Proposed multilayer inverter's fundamental component*

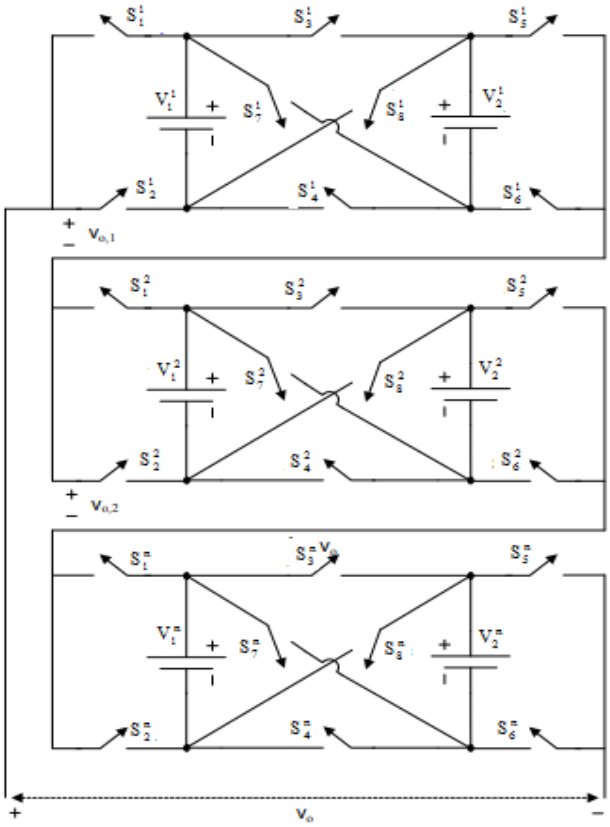

Fig. 2 *Proposed single phase cascaded multilevel inverter with 'n' units*

Table 1 *Switching table for basic unit (9-level output voltage)*

S.No.	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'	S_7'	S_8'	V_o (V_{dc}=10V)
1	1	0	1	0	0	1	0	0	$+V_{dc}$
2	1	0	0	1	1	0	0	0	$+2V_{dc}$
3	1	0	0	0	1	0	0	1	$+3V_{dc}$
4	1	0	0	0	0	1	0	1	$+4V_{dc}$
5	1	0	1	0	1	0	0	0	0
6	0	1	0	1	1	0	0	0	$-V_{dc}$
7	0	1	1	0	0	1	0	0	$-2V_{dc}$
8	0	1	0	0	0	1	1	0	$-3V_{dc}$
9	0	1	0	0	1	0	1	0	$-4V_{dc}$
10	0	1	0	1	0	1	0	0	0

Each fundamental unit can produce 9 distinct levels of output voltage ($4V_{dc}$, $3V_{dc}$, $2V_{dc}$, $1V_{dc}$, $0V_{dc}$, $-1V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$). To generate 9 levels of output voltage, the magnitude of the DC sources should be selected appropriately. If the magnitude of the DC sources in the basic unit are identical, then the level of output voltage will be equal to five. More than two basic units are cascaded together to raise the output voltage level over the 9-level. The total output voltage is expressed as:

$$V_O = V_{01} + V_{02} + V_{03} + ... + V_{0n} \quad (1)$$

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Where $V_{01}, V_{02}, V_{03}, \ldots, V_{0n}$ are output voltages of unit-1, unit-2, unit-3……. unit-n respectively. Magnitude of DC Voltage source for unit 1

$$V_1^1 = 3V_{dc} \text{ and } V_2^1 = V_{dc} \quad (2)$$

Magnitude of DC Voltage source for unit 2

$$V_1^2 = 5V_1^1 = 15V_{dc} \text{ and } V_2^2 = 5V_2^1 = 5V_{dc} \quad (3)$$

Magnitude of DC Voltage source for unit-n

$$V_1^n = 5V_1^{n-1} = 3*5^{n-1}V_{dc} \text{ and } V_2^n = 5V_2^{n-1} = 5^{n-1}V_{dc} \quad (4)$$

For the proposed multilevel inverter, the following equations can be used to determine various relations:

$N_{level} = 2*5^{n-1}$, $N_S = 8*n$ and $V_S = 2*n$

where n is number of basic units, N_{level} is level of output voltage, N_S is number of switches, V_S is number of voltage sources. In this construction, the 49 level is formed by the basic structure of 9 level multilevel inverters being coupled in cascade with one another. The output of this structure is the sum of the output of individual components that are supplied by a single-phase supply, and this capability can be extended to three-phase supplies. V_{n-1}: To get a greater level of consistency in the output voltage ratio between two dc voltage sources, V_n ought to be set to 1:5. Components needed for the unit 2, IGBT DIODE switches are referred to by the names S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{26}, S_{27}, and S_{28} respectively. There are two different voltage sources: V_{21} and V_{22}. And the value for the second unit will be as follows: V_{21} will be $5V_{11}$, and V_{22} will be $5V_{12}$. In this simulation, an RL load with values of R = 45 ohm and L = 55 mH is being employed. Figure 3 depicts the circuit diagram of a 49-level cross switched cascaded multilevel inverter. i.e.: $V_{21} = 5V_{11} = 5*30V = 150V$ and $V_{22} = 5V_{12} = 5*10V = 50V$. For each desired output, three switches from each unit will have their respective on positions activated, while the remaining switches will have their off positions taken. Cascading two nine-level units with four voltage source magnitudes results in a 1-phase output that has 49 levels. This output can be generated. The way the procedure is carried out is illustrated in the figures that follow. The red line in the figures depicts the flow of current while simultaneously generating the necessary level of voltage as the waveform for output. The highest voltage that must be present across the switches for a switch to block in the OFF position is referred to as the standing voltage. The price of the inverter will go down in tandem with the standing voltage of the switches; hence, when one switch is conducting, the other switch will either be in an off condition, or it will block the voltage.

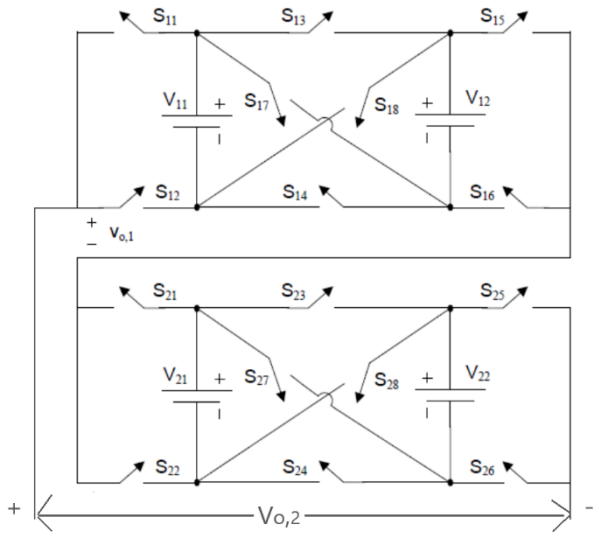

Fig. 3 *Circuit diagram of 49-Level cross switched cascaded multilevel inverter*

Modes of operation:

For +200V output: (Refer Figure 4)

The switches S_{11}, S_{13}, S_{15}, S_{21}, S_{28} and S_{26} are in ON state and the remaining switches S_{12}, S_{14}, S_{16}, S_{17}, S_{18}, S_{22}, S_{23}, S_{24}, S_{25} and S_{27} are in OFF state. The Current flow path is through $+V_o$-S_{11}-S_{13}-S_{15}-S_{21}-$(+V_{21})$-S_{28}-$(+V_{22})$-S_{26}-$(-V_o)$ and the Output voltage appeared across load terminals is +200V.

For +150V output: (Refer Figure 5)

The switches S_{11}, S_{13}, S_{15}, S_{21}, S_{24} and S_{26} are in ON state and the remaining switches S_{12}, S_{14}, S_{16}, S_{17}, S_{18}, S_{22}, S_{23}, S_{25}, S_{27} and S_{28} are in OFF state. The Current flow path is through $+V_o$-S_{11}-S_{13}-S_{15}-S_{21}-$(+V_{21})$-S_{24}-S_{26}-$(-V_o)$ and the Output voltage appeared across load terminals is +150v.

For +50V output: (Refer Figure 6)

The switches S_{11}, S_{13}, S_{15}, S_{21}, S_{23} and S_{26} are in ON state and the remaining switches S_{12}, S_{14}, S_{16}, S_{17}, S_{18}, S_{22}, S_{24}, S_{25}, S_{27} and S_{28} are in OFF state. The Current flow path is through $+V_o$-S_{11}-S_{13}-S_{15}-S_{21}-S_{23}-$(+V_{22})$-S_{26}-$(-V_o)$ and the Output voltage appeared across load terminals is +50V.

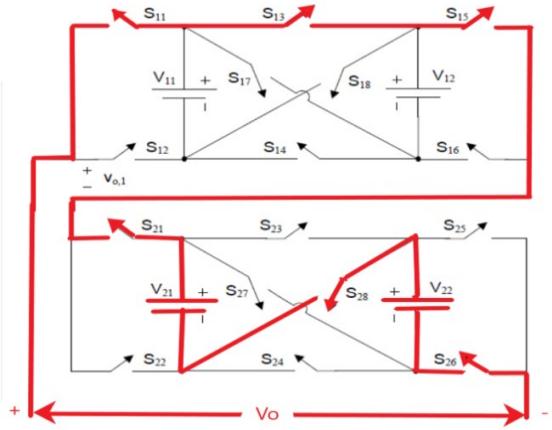

Fig. 4 *Current path of cross switched cascaded multilevel inverter for producing +200V*

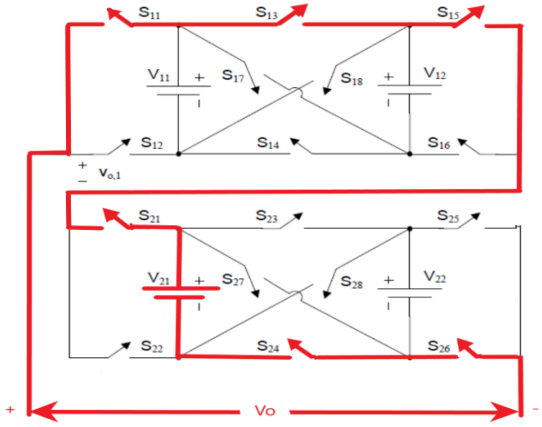

Fig. 5 *Current path of cross switched cascaded multilevel inverter for producing +150V*

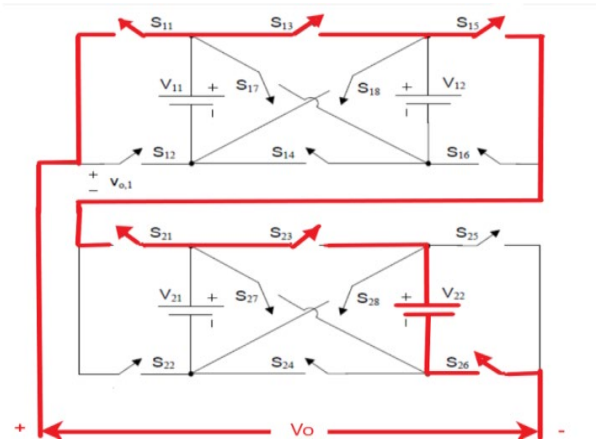

Fig. 6 *Current path of cross switched cascaded multilevel inverter for producing +50V*

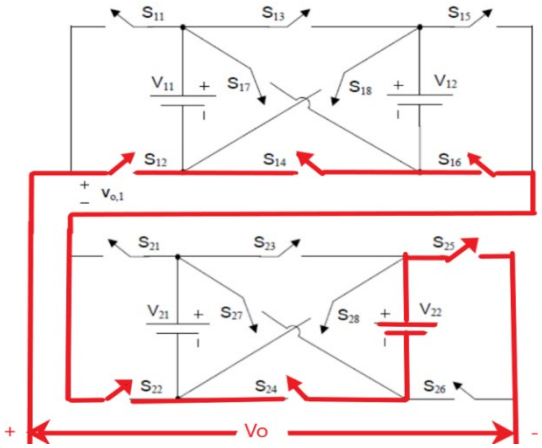

Fig. 7 *Current path of cross switched cascaded multilevel inverter for producing -50V*

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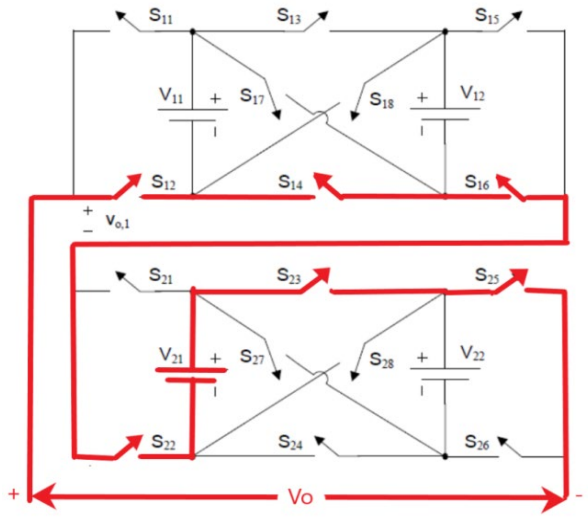

Fig. 8 *Current path of cross switched cascaded multilevel inverter for producing -150V*

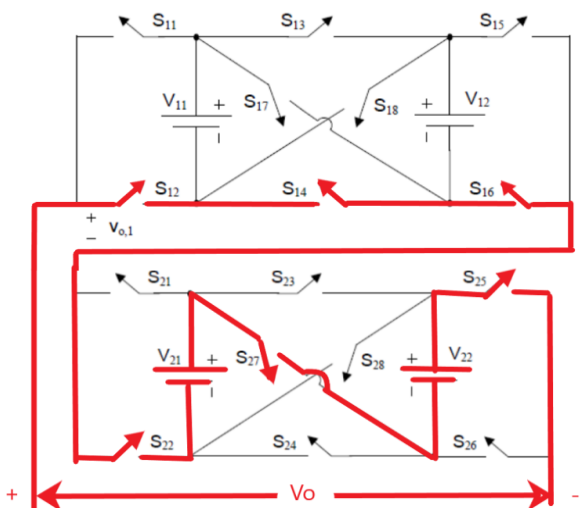

Fig. 9 *Current path of cross switched cascaded multilevel inverter for producing -200V*

For -50V output: (Refer Figure 7)

The switches S_{12}, S_{14}, S_{16}, S_{22}, S_{24} and S_{25} are in ON state and the remaining switches S_{11}, S_{13}, S_{15}, S_{17}, S_{18}, S_{21}, S_{23}, S_{26}, S_{27} and S_{28} are in OFF state. The Current flow path is through $+V_o$-S_{12}-S_{14}-S_{16}-S_{22}-S_{24}-(-V_{22})-S_{25}-(-V_o) and the Output voltage appeared across load terminals is -50V.

For -150V output: (Refer Figure 8)

The switches S_{12}, S_{14}, S_{16}, S_{22}, S_{23} and S_{25} are in ON state and the remaining switches S_{11}, S_{13}, S_{15}, S_{17}, S_{18}, S_{21}, S_{24}, S_{26}, S_{27} and S_{28} are in OFF state. The Current flow path is through $+V_o$-S_{12}-S_{14}-S_{16}-S_{22}-(-V_{21})-S_{23}-S_{25}-(-V_o) and the Output voltage appeared across load terminals is -150V.

For -200V output: (Refer Figure 9)

The switches S_{12}, S_{14}, S_{16}, S_{22}, S_{27} and S_{25} are in ON state and the remaining switches S_{11}, S_{13}, S_{15}, S_{17}, S_{18}, S_{21}, S_{23}, S_{24}, S_{26} and S_{28} are in OFF state. The Current flow path is through $+V_o$-S_{12}-S_{14}-S_{16}-S_{22}-(-V_{21})-S_{27}-(-V_{22})-S_{25}-(-V_o) and the Output voltage appeared across load terminals is -200V.

2.1 Total Standing Voltage (TSV)

Total standing voltage is also one of the important parameters to calculate the rating and cost of the switches used in multilevel inverter is standing voltage.

Unit-1

Standing voltage of switch S_1^2,S_2^2,S_3^2 and S_4^2 is $V_1^1=3V_{dc}$

Standing voltage of switch S_5^1 and S_6^1 is $V_2^1=V_{dc}$

Standing voltage of switch S_7^1 and S_8^1 is $V_2^1+V_1^1=4V_{dc}$

Total standing voltage of unit 1 is computed as

$$TSV_1 = V_1^1 + V_1^1 + V_1^1 + V_1^1 + V_2^1 + V_2^1 + V_2^1 + V_1^1 + V_2^1 + V_1^1 \quad (5)$$

$$TSV_1 = 2\left(3V_1^1+2V_2^1\right)$$

$$TSV_1 = 22V_{dc}$$

Unit-2

Standing voltage of switch S_1^2,S_2^2,S_3^2 and S_4^2 is $V_1^2=15V_{dc}$

Standing voltage of switch S_5^2 and S_6^2 is $V_2^1=5V_{dc}$

Standing voltage of switch S_7^2 and S_8^2 is $V_2^2+V_1^2=20V_{dc}$

Total standing voltage of unit 2 is computed as follows

$$TSV_2 = V_1^2 + V_1^2 + TSV_2 = V_1^2 + V_1^2 + V_1^2 + V_1^2 + V_2^2 + V_2^2 + V_2^2 + V_1^2 + V_2^2 + V_1^2 \quad (6)$$

$$TSV_2 = 2\left(3V_1^2 + 2V_2^2\right) = 5*2\left(3V_1^1 + 2V_2^1\right)$$

$$TSV_2 = 5*22V_{dc}$$

Similarly, TSV of unit-n (TSV_n) = $5^{n-1}*2\left(3V_1^1 + 2V_2^1\right)$ (7)

The TSV of n units in the proposed multilevel inverter is

$TSV = TSV_1 + TSV_2 + \ldots\ldots\ldots\ldots + TSV_n$

$$TSV = \left(1 + 5 + 5^2 + 5^3 + \ldots + 5^{n-1}\right) * 2\left(3V_1^1 + 2V_2^1\right)$$

It is essential to be aware that the selection of appropriate magnitudes for dc voltage sources is the driving force behind the existence of all possible voltage levels at the output. The primary goal of the novel cascaded multilevel inverter that has been proposed is to enhance the number of output voltage levels while simultaneously reducing the total number of components that are required. A comparison between the proposed Cross Switched Cascade Multilevel Inverter and the cascaded multilevel inverter is carried out in order to investigate the performance of the proposed topology from the points of view of the number of different voltage amplitudes of the used sources, the amount of blocked voltage, the number of IGBTs, and the dc voltage sources. This comparison is carried out in order to investigate the performance of the proposed topology. The comparison in table 3 demonstrates that the number of used power switches in the proposed topology is not only lower than the topologies with bidirectional switches, but it is also lower than the topologies with unidirectional ones. This is because the number of used power switches in the proposed topology uses only unidirectional switches. As a consequence of this, the topology that was presented had better features from this vantage point.

Table 2 *Switching table for proposed 49-level multilevel inverter*

S.No	S_1^1	S_2^1	S_3^1	S_4^1	S_5^1	S_6^1	S_7^1	S_8^1	S_1^2	S_2^2	S_3^2	S_4^2	S_5^2	S_6^2	S_7^2	S_8^2	V_o
1	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	$+24V_{dc}$
2	1	0	0	1	0	1	0	0	1	0	0	0	0	1	0	1	$+23V_{dc}$
3	1	0	0	1	1	0	0	0	1	0	0	0	0	1	0	1	$+22V_{dc}$
4	1	0	1	0	0	1	0	0	1	0	0	0	0	1	0	1	$+21V_{dc}$
5	1	0	1	0	1	0	0	0	1	0	0	0	0	1	0	1	$+20V_{dc}$
6	1	0	0	0	0	1	0	1	1	0	0	1	0	1	0	0	$+19V_{dc}$
7	1	0	0	1	0	1	0	0	1	0	0	1	0	1	0	0	$+18V_{dc}$
8	1	0	0	1	1	0	0	0	1	0	0	1	0	1	0	0	$+17V_{dc}$
9	1	0	1	0	0	1	0	0	1	0	0	1	0	1	0	0	$+16V_{dc}$
10	1	0	1	0	1	0	0	0	1	0	0	1	0	1	0	0	$+15V_{dc}$
11	1	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	$+14V_{dc}$
12	1	0	0	1	0	1	0	0	1	0	0	1	1	0	0	0	$+13V_{dc}$
13	1	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	$+12V_{dc}$
14	1	0	1	0	0	1	0	0	1	0	0	1	1	0	0	0	$+11V_{dc}$
15	1	0	1	0	1	0	0	0	1	0	0	1	1	0	0	0	$+10V_{dc}$
16	1	0	0	0	0	1	0	1	1	0	1	0	0	1	0	0	$+9V_{dc}$
17	1	0	0	1	0	1	0	0	1	0	1	0	0	1	0	0	$+8V_{dc}$
18	1	0	0	1	1	0	0	0	1	0	1	0	0	1	0	0	$+7V_{dc}$
19	1	0	1	0	0	1	0	0	1	0	1	0	0	1	0	0	$+6V_{dc}$
20	1	0	1	0	1	0	0	0	1	0	1	0	0	1	0	0	$+5V_{dc}$
21	1	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	$+4V_{dc}$
22	1	0	0	1	0	1	0	0	0	1	0	1	0	1	0	0	$+3V_{dc}$
23	1	0	0	1	1	0	0	0	0	1	0	1	0	1	0	0	$+2V_{dc}$
24	1	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	$+1V_{dc}$
25	1 0	0 1	1 0	0 1	1 0	0 1	0 0	0 0	0 1	1 0	0 1	1 0	0 1	1 0	0 0	0 0	$0V_{dc}$
26	0	1	0	1	1	0	0	0	1	0	1	0	1	0	0	0	$-1V_{dc}$
27	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	$-2V_{dc}$
28	0	1	1	0	1	0	0	0	1	0	1	0	1	0	0	0	$-3V_{dc}$
29	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0	0	$-4V_{dc}$

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30	0	1	0	1	0	1	0	0	0	1	0	1	1	0	0	0	$-5V_{dc}$
31	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	$-6V_{dc}$
32	0	1	1	0	0	1	0	0	0	1	0	1	1	0	0	0	$-7V_{dc}$
33	0	1	1	0	1	0	0	0	0	1	0	1	1	0	0	0	$-8V_{dc}$
34	0	1	0	0	1	0	1	0	0	1	0	1	1	0	0	0	$-9V_{dc}$
35	0	1	0	1	0	1	0	0	0	1	1	0	0	1	0	0	$-10V_{dc}$
36	0	1	0	1	1	0	0	0	0	1	1	0	0	1	0	0	$-11V_{dc}$
37	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	$-12V_{dc}$
38	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0	$-13V_{dc}$
39	0	1	0	0	1	0	1	0	0	1	1	0	0	1	0	0	$-14V_{dc}$
40	0	1	0	1	0	1	0	0	0	1	1	0	1	0	0	0	$-15V_{dc}$
41	0	1	0	1	1	0	0	0	0	1	1	0	1	0	0	0	$-16V_{dc}$
42	0	1	1	0	0	1	0	0	0	1	1	0	1	0	0	0	$-17V_{dc}$
43	0	1	1	0	1	0	0	0	0	1	1	0	1	0	0	0	$-18V_{dc}$
44	0	1	0	0	1	0	1	0	0	1	1	0	1	0	0	0	$-19V_{dc}$
45	0	1	0	1	0	1	0	0	0	1	0	0	1	0	1	0	$-20V_{dc}$
46	0	1	0	1	1	0	0	0	0	1	0	0	1	0	1	0	$-21V_{dc}$
47	0	1	1	0	0	1	0	0	0	1	0	0	1	0	1	0	$-22V_{dc}$
48	0	1	1	0	1	0	0	0	0	1	0	0	1	0	1	0	$-23V_{dc}$
49	0	1	0	0	1	0	1	0	0	1	0	0	1	0	1	0	$-24V_{dc}$

Table 3 *Comparative results for 49-level multilevel inverter*

Inverter Type	DC sources	Driver Circuits	Main Switches
NPC	48	96	96
Flying capacitor	48	96	96
Cascaded H-bridge	24	96	96
Proposed	4	16	16

3. Results & Discussions

The motor is controlled utilizing a power electronics interface, specifically a sinusoidal pulse width modulation (SPWM) inverter, which employs a constant voltage-to-frequency (V/f) control technique. The amplitude and frequency of the reference signals will vary based on the intended output speed. To ensure a consistent magnetic flux within the motor, it is necessary to maintain a constant ratio between the amplitude and frequency of the voltage. Therefore, an IPD-based PWM controller is employed to effectively regulate the speed of the motor to the appropriate set point. The speed control system is defined by the evaluation of the precise motor speed, which is then compared to the desired speed, resulting in the generation of an error signal. The error signal's size and polarity are indicative of the disparity between the current speed and the desired speed. The controller produces the adjusted motor stator frequency in order to rectify the discrepancy, which is determined by the deviation in speed. Simulation of the proposed 49-level multilevel inverter is performed in MATLAB/SIMULINK environment with two units connected in cascaded and induction motor as load. Various parameters that are set to the simulation are $V_{dc} = 10V$, voltage sources values of unit-1 are considered as $V_1^1 = 30V, V_2^1 = 10V$, similarly, voltage sources values of unit-2 are considered as $V_1^2 = 150V, V_2^2 = 50V$.

The output phase voltage, as illustrated in Figure 10, is represented by a digital simulation. The simulation reveals a total of 49 levels from peak to peak. Figure 10 displays a graph depicting 24 levels within the positive cycle, 24 levels within the negative cycle, and a single level representing zero potential. Figure 12 illustrates the associated total harmonic distortion (THD) for the single-phase output voltage, whereby the total harmonic distortion is claimed to be 0.38%. Figures 13 and 14 depict the phase currents and output voltage of the multilayer inverter, respectively. The amplitude of the alternating current waveform is determined to be 15A, while the peak voltage is recorded as 210V. The phase of each of the three outputs is altered by 120 degrees. The line voltage between units 1 and 2 is also observed and depicted in figures 15 and 16, respectively. The performance of the induction motor is determined by examining the output voltages and currents of the multilayer inverter in terms of line and phase. The induction motor took 0.2 seconds to stabilize due to inverter instability and oscillations; after 0.2 seconds, the speed of the machine is maintained constant, as shown in figure 17.

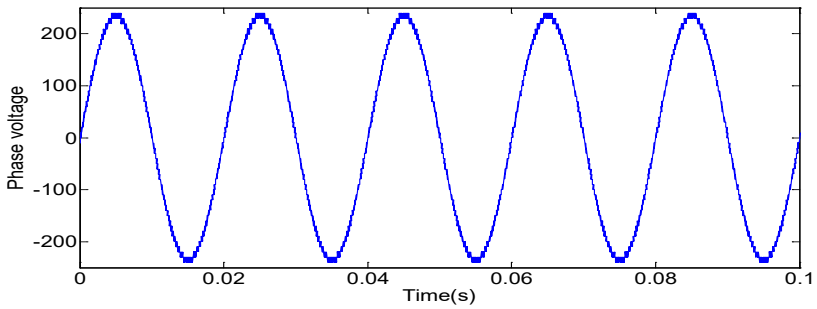

Fig. 10 *Output phase voltage of 49-level cross switched cascaded multilevel inverter*.

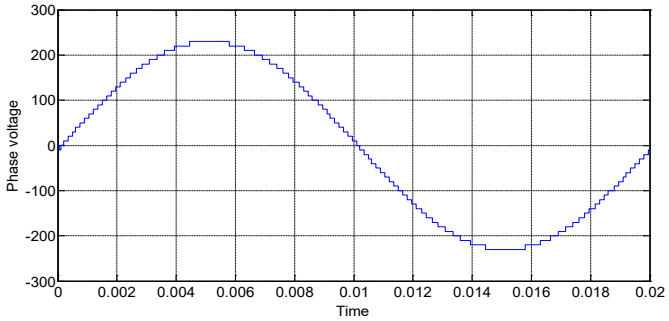

Fig. 11 *Output phase voltage of 49 level CSCMI (zoomed for one cycle)*

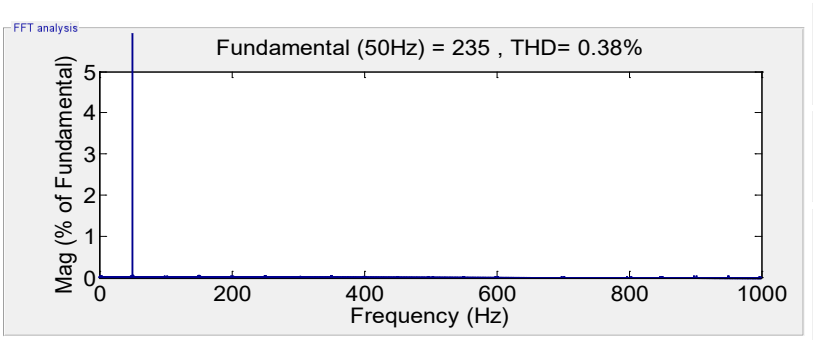

Fig. 12 *Total harmonic distortion of 49 level CSCMI output voltage*

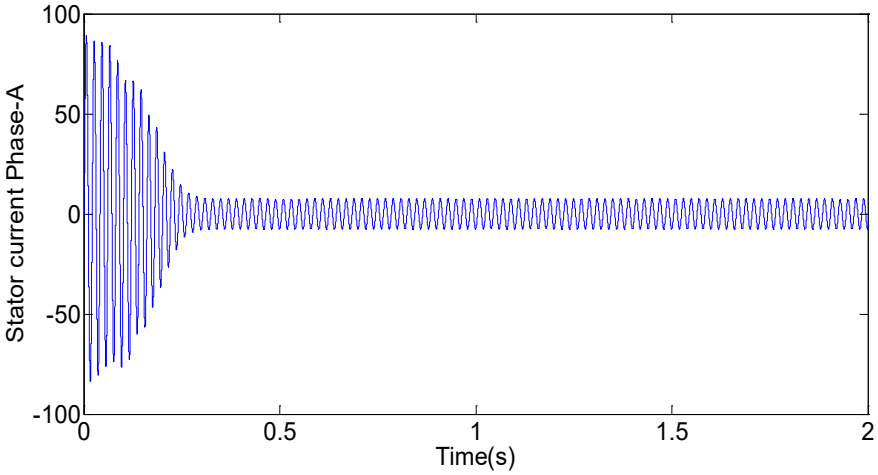

Fig. 13 *Phase current of induction machine*

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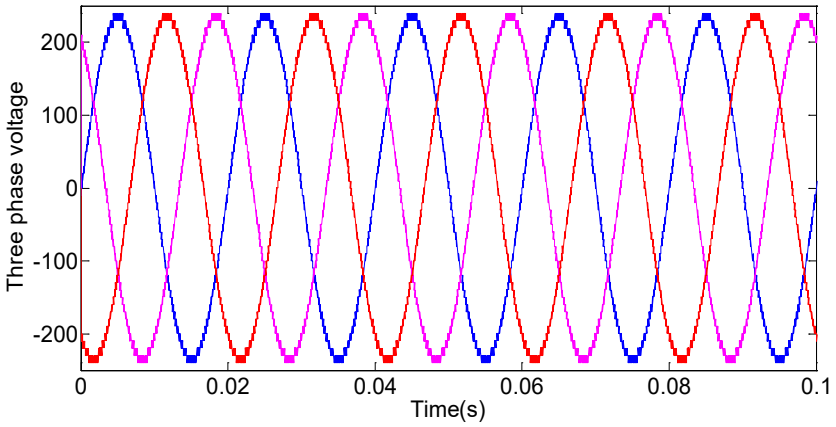

Fig. 14 *Three phase output voltage of 49 level CSCMI*

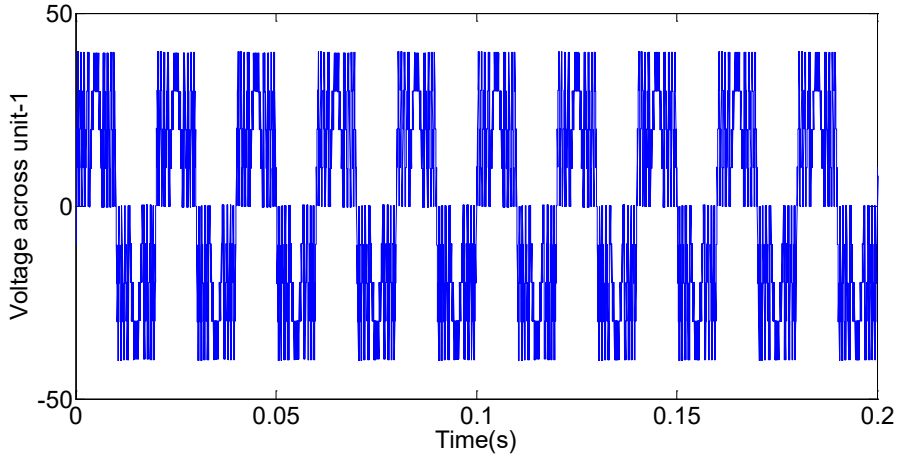

Fig. 15 *Voltage across unit 1*

4. Conclusion

The proposed topology enhances the design flexibility and expands the potential for optimizing the converter to achieve diverse aims. Research has demonstrated that the structure, including multi-level inverters (MLIs) with two switches, has the lowest switch count among various configurations for a specific quantity of voltage levels. The findings have demonstrated that the suggested topology offers a total of 49 levels for the output voltage. The proposed topology exhibits a reduced number of switches and components in comparison to alternative topologies. Additionally, its complete bridge converters work at lower voltage levels. The findings of the simulation conducted on a 49 level cross connected cascaded inverters are reported. The utilization of the cross connected cascaded multi-level inverter results in a mere 0.38% of the overall harmonic distortion being seen. The performance parameters of induction motors, including output voltage, current settling time, and speed, are significantly enhanced in the context of cross-connected cascaded multilevel inverters.

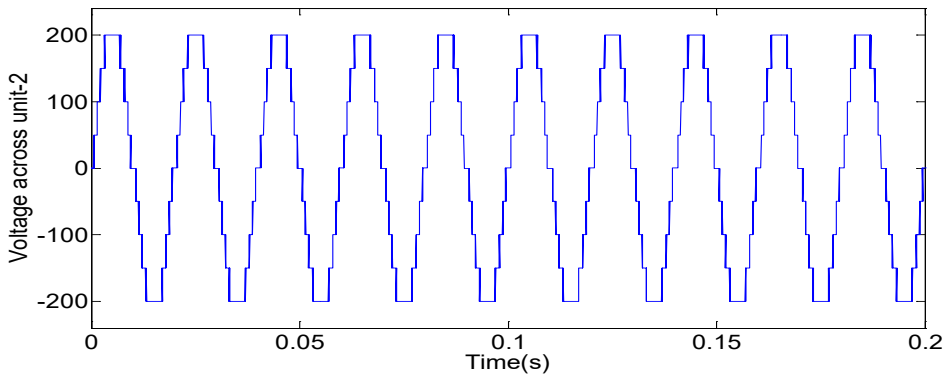

Fig. 16 *Voltage across unit 2*

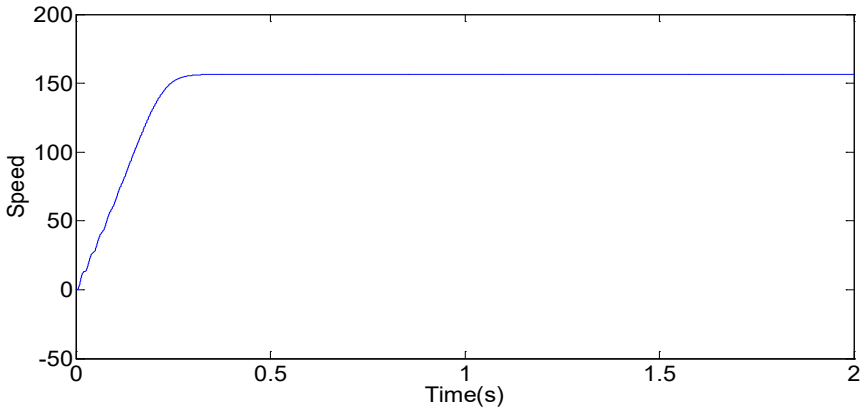

Fig. 17 *Speed of induction machine*

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

References

[1] P. Omer, J. Kumar and B. S. Surjan (2020). A Review on Reduced Switch Count Multilevel Inverter Topologies. IEEE Access, 8, 22281-22302. https://doi.org/10.1109/ACCESS.2020.2969551

[2] E.Babaei, C. Buccella, M. Saeedifard (2016). Recent Advances in Multilevel Inverter and their Applications: Part I. IEEE Transactions on Industrial Electronics, 63(11), 7145-7147. https://doi.org/10.1109/TIE.2016.2602270

[3] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama (2010). A survey on neutral point clamped inverters. IEEE Transactions on Industrial Electronics, 57(7), 2219–2230. https://doi.org/10.1109/TIE.2009.2032430

[4] M. M. Shobini, J. Kamala and R. Rathna. (2017). Analysis and simulation of flying capacitor multilevel inverter using PDPWM strategy. International Conference on Innovative Mechanisms for Industry Applications, Bangalore. https://doi.org/10.1109/ICIMIA.2017.7975578

[5] M. Pamujula, A. Ohja, R. D. Kulkarni and P. Swarnkar (2020). Cascaded 'H' Bridge based Multilevel Inverter Topologies: A Review. International Conference for Emerging Technology, Belgaum, India, 1-7. https://doi.org/10.1109/INCET49848.2020.9154031

[6] M. Sarbanzadeh, M. A. Hosseinzadeh, E. Sarbanzadeh, L. Yazdani, M. Rivera, and J. Riveros. (2018). New fundamental multilevel inverter with reduced number of switching elements. IEEE Southern Power Electronics Conference SPEC 2017. https://doi.org/10.1109/SPEC.2017.8333666

[7] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon (2019). A New Multilevel Inverter Topology with Reduce Switch Count. IEEE Access, 7, 58584–58594. https://doi.org/10.1109/ACCESS.2019.2914430

[8] V. V. Nagi Reddy, D. V. A. Kumar, and V. R. Kota (2019). A multilevel UPQC for voltage and current quality improvement in distribution system. International Journal of Power Electronic Drive Systems, 10(4), 1932-1943. https://doi.org/10.11591/ijpeds.v10.i4.pp1932-1943

[9] J. Surya Kumari, D. Lenine, A. Satish, T. Suresh Kumar, C. Kalaivani, M. Dilip Kumar, G. Kumara Swamy, Y. Vijaya Suresh, J. Nagarjuna Reddy, J. Kanna Kumar, Y. Mallikarjuna Rao (2022). A model predictive Goertzel algorithm based active islanding detection for grid integrated photovoltaic systems. Microprocessors and Microsystems, 95, 104706, https://doi.org/10.1016/j.micpro.2022.104706.

[10] E. Najafi and A. H. M. Yatim (2012). Design and implementation of a new multilevel inverter topology. IEEE Transactions on Industrial Electronics, 59(11), 4148-4154. https://doi.org/10.1109/TIE.2011.2176691

[11] M. A. Hosseinzadeh, M. Sarbanzadeh, J. Munoz, M. Rivera, C. Munoz, and A. Villalon (2019). New reduced switched multilevel inverter for three-phase grid-connected PV system, performance evaluation. IEEE International Conference in Industrial Technologies, 1488–1493. https://doi.org/10.1109/ICIT.2019.8755112

[12] K. Thakre, K. B. Mohanty, V. Kommukuri and R. N. Mishra (2017). Symmetrical and asymmetrical multilevel inverter using less number of switches. TENCON IEEE Region 10 Conference, Penang, 1032-1036. https://doi.org/10.1109/TENCON.2017.8228009
[13] B. Mahato, S. Mittal and P. k. Nayak (2018). Generalized Symmetrical/Asymmetrical Single-phase MLI Topology. International Conference on Recent Trends in Electrical, Control and Communication, Malaysia, Malaysia, 182-187. https://doi.org/10.1109/RTECC.2018.8625642
[14] D. A. B. Zambra, C. Rech and J. R. Pinheiro (2010). Comparison of Neutral-Point-Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters. IEEE Transactions on Industrial Electronics, 57(7), 2297-2306. https://doi.org/10.1109/TIE.2010.2040561
[15] J. Srinivas Rao, P. Srinivasa Varma, T. Suresh Kumar (2018). Novel Switching Design Structure for Three Phase 21-Level Multilevel Inverter Fed BLDC Drive Application. International Journal of Power Electronics and Drive System, 9(3), 1202-1213. https://doi.org/10.11591/ijpeds.v9.i3.pp1202-1213
[16] A. Anan, T. K. Chakraborty, and K. Sultan Mahmood (2018). A Single-Phase Cascaded H-Bridge Multilevel Inverter with Reduced Switching Devices and Harmonics. 6th IEEE International Conference on Smart Energy Grid Engineering, 222–225. https://doi.org/10.1109/SEGE.2018.8499512
[17] S. K. Tummala and L. Duraiswamy. (2022) Switched Mode Power Supply: A High Efficient Low Noise Forward Converter Design Topology. IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT), Hyderabad, India, pp. 1-5, https://doi.org/10.1109/SeFeT55524.2022.9908809.
[18] Kamaldeep Boora, Jagdish Kumar (2016). A New Cross Switched Cascaded Multilevel Inverter Topology with Reduced Number of Switches. IEEE 7th Power India International Conference (PIICON). https://doi.org/10.1109/POWERI.2016.8077426