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# Modelling and Characterization of a 14 nm Planar p-Type MOSFET Device

**Noor Faizah Z. A.[1], I. Ahmad[1*], P.J.Ker[1], and P.S. Menon[2].**

[1] Centre for Micro and Nano Engineering (CeMNE), Universiti Tenaga Nasional (UNITEN)
43009 Kajang, Selangor, Malaysia.

[2] Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM)
43600 Bangi, Selangor, Malaysia.

**Abstract:** Coined by Gordon E. Moore through its law, a proper scaling is enforced for optimum device performance. Since 2k millennium, technology of metal gate on high-k dielectric was introduced to reduce the impact of scaling ultimatum on a transistor. In this letter, a 14nm planar p-type MOSFET device is virtually fabricated using ATHENA module and characterized for its performance evaluation using ATLAS module where both can be found in Virtual Wafer Fabrication (VWF) of Silvaco TCAD Tools. This is the continuance research from our established 32nm device simulation using $HfO_2/TiSi_2$. The findings show that the optimal value of threshold voltage ($V_{TH}$), drive current ($I_{ON}$) and leakage current ($_{IOFF}$) are -0.231507V, 72.4534 µA/um and 6.58635 pA/um respectively. The performance results also present a good switching capability of the device since the $I_{ON}/I_{OFF}$ ratio value is $\approx 10^6$. The results of this work demonstrate that this 14nm planar p-type device possesses a good performance which can workhorse to future design and optimization.

**Keywords:** 14nm p-type transistor, high-k dielectrics, metal gate, $HfO_2$, $TiSi_2$, Silvaco TCAD Tools.

## 1. Introduction

Late 1970s was the touchstone of devices' energy conservation. It is when the semiconductor industry responded aggressively towards the principle of scaling published by R. Dennard [1]. The goal is to achieve high integration density in a single chip which will results in higher transistor drive current and lowering the production cost at once. Unfortunately, at film thickness less than 1.5nm, the conventional $SiO_2$/Poly-Si MOSFET suffers from leaky gate oxide. Other problems such as short channel effect (SCE) and drain induced barrier lowering (DIBL) [2, 3] may affect the device performance negatively due to high power consumption. It could be easily predicted that if there was no new invention, a conventional MOSFET with an extremely small gate length down to 5nm may have performance that is shoddier than 20nm gate length.

Innovations on device structure and variation of material to replace conventional $SiO_2$/Poly-Si were then introduced to overcome the conventional MOSFET detriment and at once, enhance the device performance. These efforts include the replacement of materials $SiO_2$ to high-k dielectric and Poly-Si gate to metal gate and different structures such as double gate and FinFET. These inventions are needed to allow rapid scaling and to design not only a small transistor that switches fast but has enormously small $I_{OFF}$ when it is turned off. Furthermore, a $V_{TH}$ that is not too dependent on gate length, device does not suffer too much from parameter-induced fluctuations, and the possibility of devices to be interconnected three dimensionally with multiple levels of wiring are also the major advantages of downscaling of MOSFET devices. To date, MOSFETs with a minimum of 15nm gate lengths have been analyzed and demonstrated. A small 12nm and 14nm gate length modified double gate transistor which still utilized the conventional $SiO_2$/Poly-Si is discussed in [4] and [5] while paper in [6] discussed on a performance of 14nm gate length transistor utilizing a SOI FinFET structure. Regardless of a very small gate length, their design proved that the downscaling of a transistor is conceivable besides showing a promising performances character which can be set as a benchmark for advance research analysis.

In our research, the design of planar 14nm p-type transistor is downscaled from the established 32nm transistor where the paper can be found in [7]. For simplicity, the same high-k metal gate materials are employed in this research using Hafnium Dioxide ($HfO_2$) as an insulator and Titanium Silicide ($TiSi_2$) as a metal gate. In addition, it is to attest that the downscaled of a transistor from 32nm to 14nm gate length is not only possible but achievable. The criteria of choosing $HfO_2$ has been discussed in [8] where it is said to be advantageous in achieving a low leakage current. $TiSi_2$ on the other hand is chosen as it is capable to deliver high drive current ($I_{ON}$) when a proper retrograde channel is used [7]. However, a proper scaling on the device and accurate doping concentrations should also be considered as it will severely affect the device performance.

*Corresponding author: AIbrahim@uniten.edu.my
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A comprehensive study was carried out to investigate the device performance before the optimization process can be done in future research. The outcomes are as presented in this letter and it is achieved by executing variations in several implantation dosages of process parameters. A 14nm-long $HfO_2/TiSi_2$ gate was virtually patterned successfully within the International Technology Roadmap for Semiconductor (ITRS 2013) prediction. From the ITRS 2013 [10], $V_{TH}$ should be within ±12.7% of 0.230 V, drive current ($I_{ON}$) is expected to be equal to or more than 1267µA/um for excellent driving capability of MOSFET device [4] and $I_{OFF}$ is expected to be equal or less than 100nA/um for excellent suppression of SCE. Despite of the tremendously fine gate, this device also exhibits an excellent $I_{ON}/I_{OFF}$ ratio. The structure of the paper is organized as follows: Section II clarifies the scaling procedure, Section III discovers the experimental materials and methods, Section IV discusses the device's performance analysis, and Section V summarizes the paper.

## 2. Scaling Procedure

Scaling is introduced back then to respond to the Moore's Law besides maximizing the device performance as well as to meet the demands in mobile communication and computation technology. Scaling can be done using the scaling method stated in [11]. It suggests that the horizontal and vertical dimensions are scaled down using the same factor, α and the Si-substrate impurity concentration is increased. This trend is also accelerated by every update of the ITRS due to severe competitions between the rival Large Scale Integrated (LSI) device to produce such high performance device. The formula for scaling is;

$$\beta = \frac{1}{\alpha} \quad (1)$$

where α = 32nm/14nm, representing the ratio of 32nm gate length to 14nm gate length, and β=0.4375. The device dimension and mesh setting are scaled down accordingly using the ratio value.

## 3. Experiment Descriptions

### 3.1 Virtual fabrication of p-type MOSFET using ATHENA Module

14nm p-type transistor was virtually design using 2D ATHENA module. It was where all the virtual deposition, implantation, etching, and annealing take place and analyzed for its doping profile. Since the design processes were scaled based on our previous experiments [7-12], the design structure which utilized HfO2/$TiSi_2$ materials is the same except on several parameters such as the level of doping concentration, energy and tilting angle due to the difference in size and gate length of the transistor. The summarized process data of 14nm p-type transistor design is shown in Table 1.

Table 1 p-type MOSFET fabrication recipe

| **Process Step** | **p-type MOSFET Parameters** |
|---|---|
| Silicon substrate | • <100> orientation |
| Retrograde well implantation | • 200Å oxide screen by 970°C, 20 min of dry oxygen<br>• $4.5x10^{11}$ $cm^{-3}$ Phosphorous<br>• 30 min, 900 °C diffused in nitrogen<br>• 36 min, dry oxygen |
| STI isolation | • 130Å stress buffer by 900°C, 25 min of dry oxygen<br>• 1500Å $Si_3N_4$, applying LPCVD<br>• 1.0 um photoresist deposition<br>• 15 min annealing at 900 °C |
| Gate oxide | • diffused dry oxygen for 0.1 min, 815 °C |
| Vt adjust implant | • $1.8x10^{11}$ $cm^{-3}$ Boron difluoride<br>• 5 KeV implant energy, 7° tilt<br>• 20 min annealing at 800 °C |
| High-K/Metal gate deposition | • 0.002 um $HfO_2$<br>• 0.038 um $TiSi_2$<br>• 17 min, 900 °C annealing |
| LDD implantation | • $3x10^{13}$ $cm^{-3}$ Phosphor<br>• 20° tilt |
| Sidewall spacer deposition | • 0.008 um $Si_3N_4$ |
| S/D implantation | • $1.4x10^{13}$ $cm^{-3}$ Boron<br>• 10 KeV implant energy<br>• 7° tilt |
| PMD deposition | • 0.3 um BPSG<br>• 25 min, 850 °C annealing |
| Metal 1 | • 0.04 um Aluminum |
| IMD deposition | • 0.04 um BPSG<br>• 15 min, 950 °C annealing |
| Metal 2 | • 0.12 um Aluminum |

The virtual 14nm p-type transistor design process was considered complete once the metallization and etching processes were done and the bonding pads were opened. The virtual transistor will then undergo the electrical characteristic simulation through ATLAS module. The target was to extract the electrical characteristics from the design such as the graph of drain current ($I_D$) versus drain to source voltage ($V_{DS}$) and the graph of $I_D$ versus $V_{GS}$. It was an important procedure where the designed transistor was tested for its functionality. The device performance parameters which are $V_{TH}$, $I_{ON}$, and $I_{OFF}$ were also extracted from the

graphs. The load profile of 14nm p-type MOSFET is depicted in Fig. 1. From the figure, all the doping concentration of input parameters can be seen clearly and the separation between the source and drain can be defined accordingly.

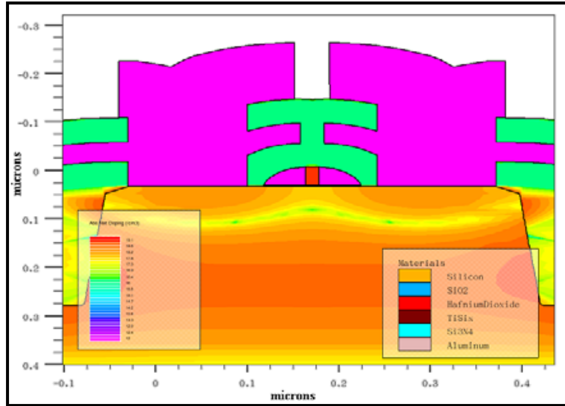


Fig.1 14nm Planar p-type MOSFET Design

### 3.2 p-Type MOSFET Characterization

The performance results of 14nm p-type MOSFET should be within the ITRS 2013 prediction. It is a guideline to follow world widely for a specific design and technology node. Thus, it is crucial to vary process parameters such as doping concentration wisely as they affect the device performance the most. In fact, a good doping concentration at certain level of energy and tilting angle would ensure that the transistor will function efficiently [2]. The input parameters which were varied in our design covers almost all parameters such as diffusing time, doping concentration, implantation energy and tilting angle. Unfortunately, the value of $V_{TH}$ and $I_{OFF}$ are trade-off; meaning that a good value of $V_{TH}$ might cause high leakage current and a lower leakage current might cause $V_{TH}$ value beyond ITRS prediction. Thus, the input parameters are varied precisely in order to get the performance results near to ITRS prediction. In this research, a high value of Halo Implant dose and Compensation Implant dose increase the $V_{TH}$ value while the increase in S/D Implant dose decreases the $V_{TH}$ value. Thus, it was observed that one increase in input parameter would compensate the other and there was an optimum point that would produce an optimum device performance.

## 4. Results and Analysis

A complete design of 14nm planar p-type MOSFET was tested for its performance analysis through ATLAS module. Graphs of electrical characterization were generated from the simulations. The electrical characterization graphs of the device are shown in Fig. 2, Fig. 3, and Fig. 4 . Fig. 2 show the graph of Drain Current ($I_{DS}$) versus Drain Voltage ($V_{DS}$) at $V_G$ = 0.5 V, 1.1 V, 2.2 V and 3.3 V, repsectively. Fig. 3 show the graph of Drain Current ($I_{DS}$) versus Gate Voltage ($V_{GS}$) at $V_D$ = 0.05 V and 0.1 V while Fig. 4 show the graph of sub-threshold $I_{DS}$ versus $V_{GS}$ at $V_D$ = 0.1 V and 1.1 V. From Fig.3, the extracted value of $V_{TH}$ is -0.231507 V and it is acceptable since the value is still within the ITRS 2013 prediction. $I_{ON}$ and $I_{OFF}$ were extracted from the sub-threshold graph shown in Fig. 4. From the graph, it can be observed that the value of $I_{ON}$ and $I_{OFF}$ are 72.45 μA/um and 6.58635 pA/um respectively. The value of $I_{ON}$ is much lower than that of ITRS prediction; however the value of $I_{OFF}$ is way better than the ITRS prediction. The details on the device performance compared to the ITRS 2013 prediction are summarized in Table 2.

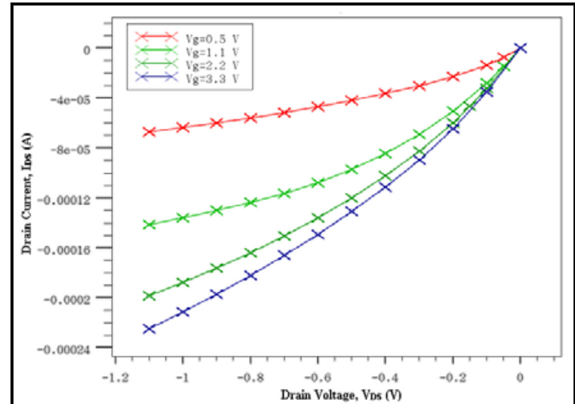


Fig.2 Graph of Drain Current ($I_{DS}$) versus Drain Voltage ($V_{DS}$)

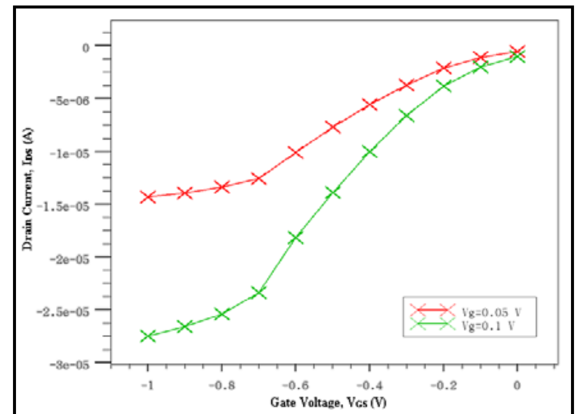


Fig.3 Graph of Drain Current ($I_{DS}$) versus Gate Voltage ($V_{DS}$)

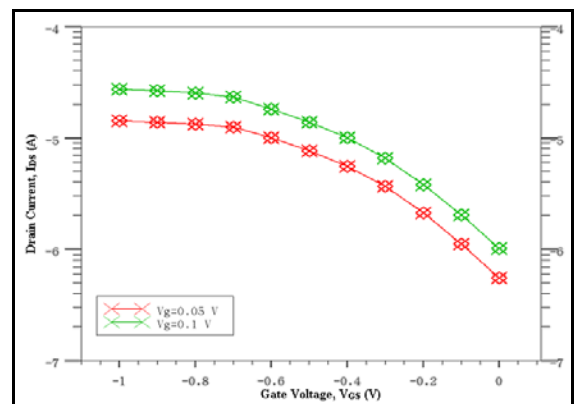


Fig.4 Graph of Sub-Threshold Drain Current ($I_{DS}$) versus Gate Voltage ($V_{GS}$)

Table 2 Simulation results as compared to ITRS 2013 prediction.

| Parameter | ITRS 2013 Prediction | Simulation Results |
|---|---|---|
| $V_{TH}$ | -0.230± 12.7% V | -0.231507 V |
| $I_{ON}$ | 1267 µA/µm | 72.4534 µA/µm |
| $I_{OFF}$ | 100 nA/µm | 6.58635pA/µm |
| $I_{ON}/I_{OFF}$ Ratio | ≈$10^3$ | ≈$10^6$ |

## 5. Summary

The design and characterization of a planar14nm p-type MOSFET which is downscaled from 32nm device was succeeded and succinctly presented. In spite of having a very small gate length, this transistor demonstrated an excellent performance with nearly zero leakage. The $V_{TH}$ value is reported to be well within the ITRS 2013 prediction and although the $I_{ON}$ is below the predicted value. Thus, the device that is presented in this work can serve as the touchstone for further research and optimization for better functionality. In short, the overall process of designing a 14nm gate length transistor is possible and achievable.

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## References

[1] R.H. Dennard, Gaesslen, H. Fritz, V.L. Rideout, E. Bassous, and A.R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," IEEE Journal of Solid-State Circuits, vol. 9(5), pp. 256-268, 1974.

[2] Fauziyah Salehuddin, Ibrahim Ahmad, Fazrena Azlee Hamid, Azami Zaharim, "Analyze and Optimize the Silicide Thickness in 45nm CMOS Technology Using Taguchi Method", IEEE-ICSE Proc., pp.19-24, 2010.

[3] H.A.Elgomati, B.Yeop Majlis, F.Salehuddin, I.Ahmad, A.Zaharim, "Cobalt Silicide and Titanium Silicide Effects on Nano Devices," IEEE-RSM Proc., pp.282-285, 2011.

[4] Khairil Ezwan Kaharudin et. All, "Design and Analysis of Ultrathin Pillar VDG-MOSFET for Low Power (LP) Technology", 8TH MUCET, Nov 2014.

[5] Hisao Kawara, Toshitsugu Sakamoto et. Al, "Transistor Characteristics of 14nm Gate Length EJ-MOSFET", IEEE Transactions on Electron Devices, vol. 47, no. 4, p. 856-860, April 2000.

[6] OushpaK, Kiran Bailey, Sowmya Sunkara, "Performance of 14nm SOI FinFET with ZrO2 dielectric: A Comparative Study", Int. Journal of Engineering Research and General Science, vol. 3, p. 299-305, 2015.

[7] Afifah Maheran A.H., Noor Faizah Z. A., P. S. Menon, I. Ahmad, P.R. Apte et. Al, "Statistical Process Modelling for 32nm High-K/Metal Gate PMOS Device" IEEE-ICSE Proc., p. 232-235, 2014.

[8] Norani Atan, I. Ahmad, B.Y. Majlis, "Effects of High-K Dielectrics with Metal Gate for Electrical Characteristics of 18 nm NMOS Device", IEEE-ICSE Proc., p. 56-59, 2014.

[9] Yongho Oh, Youngmin Kim, "Gate Workfunction Optimization of 32 nm Metal Gate MOSFET for Low Power Applications", Journal of Electrical Engineering & Technology, vol. 1, no. 2, p. 237-240, 2006.

[10] ITRS 2013 Report; http://www.itrs.net.

[11] Afifah Maheran A.H., Menon P.S., I. Ahmad, et.all, "Scaling Down of the 32 nm to 22 nm Gate Length NMOS Transistor", IEEE-ICSE Proc., p. 173-176, 2012.

[12] F.Salehuddin, I.Ahamd, F.A.Hamid, A.Zaharim, "Influence of HALO and Source/Drain Implantation on Threshold Voltage in 45nm PMOS Device", Australian Journal of Basic and Applied Sciences, pp.55-61, 2011.