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A Robust Control for Five-level Inverter Based on Integral Sliding Mode Control

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Abstract: The limitations of classical carrier wave-based pulse width modulation (PWM) techniques prevent them from ensuring good output quality for multi-level inverters. This paper proposes a new sliding mode control (NSMC) method for controlling cascaded H-bridge multi-level inverters (CHB-MLIs) to improve the output quality of the inverter, reduce the common-mode (CM) voltage with high-order harmonics, and achieve stable and robustness control for the CHB-MLIs. The NSMC method modulates the PWM pulses for the multi-level inverter by comparing the control signal u(t) and the comparator levels without using carrier wave techniques. This approach facilitates the formation of a control signal u(t) which can be flexibly adjusted to optimize the generation of PWM pulses. To reduce the chattering problem around the sliding-mode surface at high frequencies and to increase speed convergence, the integral sliding-mode surface integrated with a continuous control law is used to design the controller. Additionally, a first-order low-pass filter (LPF) with a variable cut-off frequency is added to the control law to improve stability and reduce oscillation caused by rapid and large changes in the load current amplitude. The stability of the control system is validated by the Lyapunov theory. Simulation and experimental tests were performed on the same cascaded H-bridge five-level inverter (CHB-5LI) with an R-L load. The results show that the proposed NSMC method is robust and performs better efficiently for multi-level inverter control systems. Furthermore, the output quality of the inverter is significantly improved compared to classical carrier wave-based PWM techniques, with a reduced CM voltage and fewer high-order harmonics, resulting in reduced losses and switching frequency. Therefore, the stability and strong robustness of the CHB-MLIs can be achieved by the proposed NSMC method.

Keywords: Multi-level inverters, sliding mode control, PWM modulation

1. Introduction

Multi-level inverters are presently under extensive research and application with various topologies [1-2]. Among the numerous multi-level topologies, the cascaded H-bridge multi-level inverters (CHB-MLIs) have been the focus of attention among researchers [3]. CHB-MLIs have a simple module structure that allows them to produce more voltage levels and smoother output waveforms, resulting in a lower level of output harmonic distortion compared to other multi-level topologies such as diode-clamped and flying capacitor inverters [4]. Additionally, the CHB-MLIs can operate at higher voltages due to their modular structure. The cascaded inverter can synthesize a desired voltage from several independent sources of DC voltages, making it suitable for a wide range of applications, from low-power inverters to high-voltage power transmission systems, industrial applications, renewable energy, and motor drive systems [5-6]. The modularity and flexibility of CHB-MLIs configuration in design allow for easy expansion or reduction to meet specific voltage and power requirements. The cascaded inverter structure can avoid the need for extra clamping diodes or voltage-balancing capacitors, simplifying the inverter configuration. Furthermore, because each module can work independently, topologies also have the advantage of reducing dv/dt stress on IGBTs, which can help prolong their lifespan, improving the system's reliability greatly [8]. The reliable, efficient, and flexible nature of CHB-MLIs makes them an appropriate

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choice for enhancing the stability and reliability of various systems.

Although the exceptional advantages of CHB-MLIs, the common-mode (CM) voltage phenomenon with high-order harmonic distortion at the output of the inverter is still present [9-10]. This CM voltage, which contains high-frequency components, deteriorates the output voltage quality, hastens aging, reduces reliability, and even causes system instability [11]. Additionally, the CM voltage easily affects sensitive electronic devices located nearby, resulting in electromagnetic interference that infiltrates the system and causes signal distortion [8,12]. Therefore, reducing CM voltage and improving the output quality of the inverter are crucial to enhance reliability and address industrial applications.

To mitigate the issues caused by CM voltage, pulse width modulation (PWM) techniques based on carrier wave modulation have been developed, such as in-phase disposition modulation (IPD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). However, these techniques cannot completely eliminate CM voltage or reduce harmonic distortion [9-14]. Moreover, these solutions still utilize passive filters such as coils and capacitors, increasing the size and losses of the inverter [15]. The solutions listed in references [16-18] have shown efforts to reduce CM voltage in multi-level inverters, but they still cannot completely eliminate harmonic distortion or decrease switching losses. This leads to a reduction in the overall performance of the system. Furthermore, the complex algorithms involved in these solutions increase the computation burden for memory controller units, reducing processing speed and algorithm efficiency [8,19].

The overall stability and robustness of a system depend largely on the complexity of the system in addition to the quality of the output of the inverters. Designing controllers for multivariable nonlinear systems with continuous variable changes over time and small oscillation amplitudes is a significant challenge. Moreover, it is challenging to design controllers for industrial applications that require fast response and good noise immunity [20-21]. New control theories, such as fuzzy logic control theory [22], neural networks [23], hybrid fuzzy neural [24], and sliding-mode control (SMC) [25], have been applied to design controllers for nonlinear systems. Among these theories, SMC is considered the most outstanding due to its advantages of strong robustness, good noise immunity, and high stability. SMC is a highly effective approach in different fields [26-28]. It is appropriate for motor drive applications due to its flexible implementation in inverter control [29-30]. However, the main disadvantage of the SMC method is the chattering problem around the sliding-mode surface when there is a rapid change with a large amplitude of system parameters. A large switching gain solution has been introduced to achieve the robustness of the controller [31]. This solution helps to converge quickly and reduce chattering. However, it also has the disadvantage of making the system more unstable, and the chattering problem can become more severe if noise infiltrates the system from outside [32]. In a study [33], a controller was designed to stabilize the system. However, the sliding-mode surface still used the classical linear sliding mode, so the quality of the designed controller was not guaranteed.

This article proposes a robust control method based on the new sliding mode control (NSMC) for CHB-MLIs, with the aim of improving the output quality of the inverter, reducing the CM voltage with high-order harmonics, and achieving stable and sustainable control for the CHB-MLIs. The NSMC method modulates the PWM pulses for the multi- level inverter by comparing the control signal u(t) and the comparator levels, rather than relying on carrier waves as in previous classical modulation techniques. Due to adjusting the u(t) signal, it is possible to generate PWM pulses that are more optimized. To reduce chattering around the sliding-mode surface caused by the non-continuous control law at high frequencies, the NSMC method proposes a nonlinear sliding-mode surface combined with a continuous control law. Furthermore, a first-order low-pass filter (LPF) with a variable cut-off frequency is added to the control law to increase stability and reduce oscillation caused by rapid and large changes in the load current amplitude. The proposed NSMC method ensures speedy convergence, strong robustness, and the elimination of chattering phenomena, thereby enabling the CHB-MLIs to achieve high performance by reducing CM voltage, minimum THD%, and limiting losses via decreasing switching frequency, without classical carrier wave-based PWM techniques. Simulation and experimental tests were performed on the same cascaded H-bridge five-level inverter (CHB-5LI), and the stability of the NSMC control was evaluated using the Lyapunov stability theory. The results verified the effectiveness and superiority of the proposed NSMC method.

2. System Modeling and Problem Formulation

This section presents a new robust control model for the CHB-5LI, which utilizes a unique method of generating PWM pulses. Unlike traditional approaches that rely on carrier wave modulation, this method generates PWM pulses by comparing the control signal u(t) and the comparator levels. This new PWM modulation technique enables the inverters to achieve enhanced performance and robust control of inverters without using conventional carrier wave PWM modulation. Consequently, this innovative approach improves the features of the inverter, leading to a significant enhancement in performance.

2.1 Model of Cascaded Multi-Level Inverter with R-L Load

With their simple structure, CHB-MLIs can be composed of two or more H-bridge cells, allowing for easy separation of DC voltage sources. This study will focus on the CHB-5LI, which utilizes two H-bridge cells and eight IGBT switches.

In addition, the R-L load model is also considered for the CHB-5LI. The model of single-phase CHB-5LI with the

R-L load can be illustrated in Fig. 1(a) and Fig. 1(b), respectively. The mathematical model of R-L load can be expressed as follows

$$\begin{cases} u(t) = L\frac{\mathrm{d}i_x(t)}{\mathrm{dt}} + \mathrm{R}i_x(t) \\ x = \mathrm{a}, \mathrm{b}, \mathrm{c} \end{cases} \quad (1)$$

where R and L are the resistor and inductor, respectively; u(t) is the output voltage of the inverter; $i_x(t)$ is the load current; and a, b, c are phase a, b and c, respectively.
The current $i_x(t)$ can be given by

$$\begin{cases} i_x(t) = \frac{2}{3}(i_a + \mathrm{a}i_b + a^2 i_c) \\ a = e^{j\frac{2\pi}{3}} \end{cases} \quad (2)$$

The CM voltage is generated by the switching states of the IGBTs. It can be determined as

$$\begin{cases} V_{\mathrm{cm}} = \frac{V_{\mathrm{ao}} + \mathrm{V_{bo}} + \mathrm{V_{co}}}{3} \\ S_{\mathrm{xj}} + \mathrm{S'_{xj}} = 1; \mathrm{j} = 1, 2, \ldots \mathrm{n}\text{-}1 \end{cases} \quad (3)$$

where V_{ao} refers to the voltage between phase a and 0 point; phases b and c are similar.

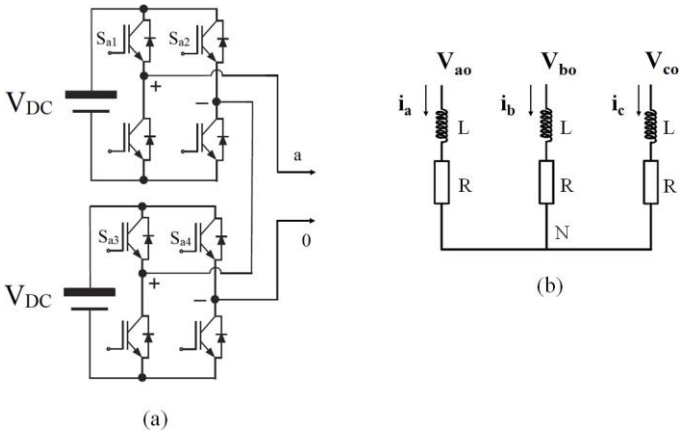


Fig. 1 - (a) The structure diagram of single-phase CHB-5LI; (b) R-L load model

2.2 Pulse Width Modulation Technique

Increasing the number of levels and choosing the proper modulation techniques can improve the output quality of inverters. The sequencing of switching is determined by the PWM technique, where the carrier wave is compared to a reference signal, and based on this comparison, the gating signal and switching time are determined. While different PWM methods have been developed over time to enhance the performance of inverters, methods based on carrier wave techniques such as IPD, APOD, or POD cannot effectively reduce CM voltage, total harmonic distortion, and switching losses. Therefore, a new method called NSMC has been proposed for the CHB-5LI. The NSMC method generates PWM pulses using the control signal u(t) from the output signal of the NSMC controller, which is compared to the comparator levels denoted as "nLevel". The general structure diagram of the proposed model is illustrated in Fig. 2. Compared to previous methods, the NSMC method uses a different approach to generate PWM pulses without relying on conventional carrier wave techniques. The reference currents of three-phase a, b, and c are applied with the value i^* = i^* .The control signal u(t) can be obtained through the NSMC method and discussed in section 3.

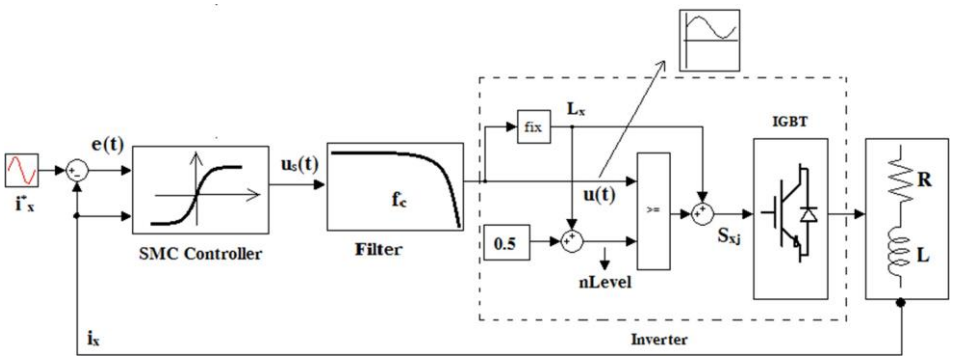


Fig. 2 - Schematic diagram of the robust control model for the CHB-5LI

Assuming $x = a, b, c$ and n level of the inverter, the control signal $u(t)$ is given as

$$0 \le u(t) \le (n-1) \tag{4}$$

To determine the instantaneous value of the signal $u(t)$ when $u(t)$ can be changed, a quantum signal L_x is given as

$$0 \le L_x \le \text{n-2} = \begin{cases} \text{n -2, when } u(t) \ge \text{n-2} \\ \text{fix}(u(t)), \text{else} \end{cases} \tag{5}$$

The comparator levels can be expressed as

$$\text{nLevel} = L_x + 0.5 \tag{6}$$

Comparison between the control signal u(t) and the comparator levels with n = 5 can be expressed in Fig. 3.

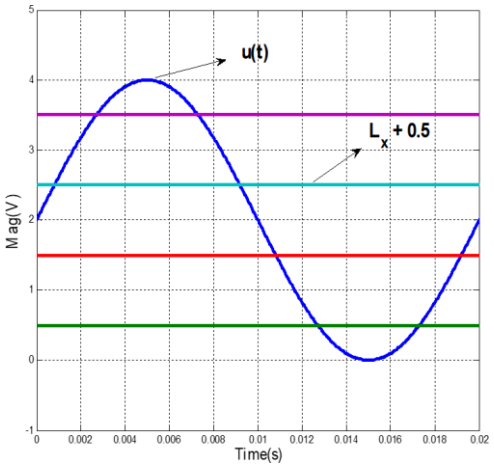


Fig. 3 - Control signal u(t) and comparator levels

Furthermore, S_{xjj} with $x = a, b, c$ and $jj = 1,2, \dots, n-1$ are the switching states of IGBTs. When the voltage of the H-bridge inverter is V_{dc}, the values of the output voltage can be obtained in the range $-2V_{dc}$, $-1V_{dc}$, 0, $+1V_{dc}$, and $+2V_{dc}$.The switching states of phase a and the output voltage values of the inverter can be shown in Table 1.

Table 1 - The switching states of phase a

S_{xxx}	$S_{aaa}\,S_{aaa}\,S_{aaa}\,S_{aaa}$	**Output voltage**
0	[0,1,0,1]	-2 V_{dc}
1	[0,0,0,1]; [1,1,0,1]; [0,1,1,1]; [0,1,0,0]	-1 V_{dc}
2	[0,0,0,0]; [1,1,1,1]; [1,1,0,0]; [0,0,1,1]; [0,1,1,0]; [1,0,0,1]	0 V_{dc}
3	[1,0,0,0]; [0,0,1,0]; [1,1,1,0]; [1,0,1,1]	+1 V_{dc}
4	[1,0,1,0]	+ 2 V_{dc}

The CM voltage will not be produced if S_{xjj} is satisfied as follows

$$\begin{cases} L_{\min} \le \sum_{x\,=\,a,b,c} S_{xj} \le L_{\max} \\ L_{\min} = 1.5n - 2.5 \\ L_{\max} = L_{\min} + 2 \end{cases} \tag{7}$$

where n is the level of an inverter.

In conventional POD modulation, the PWM pulses can be produced through the multi-level alteration of the carrier signal (V_{carr}). In this case, the PWM is determined as

$$\text{PWM} = \begin{cases} 1, \text{ when } V_{\sin}(t) \ge V_{\text{carr}} \\ 0, \text{ else} \end{cases} \tag{8}$$

Meanwhile, the proposed NSMC method can generate the PWM pulses through the control law u(t) with comparator levels. Fig. 4(b) shows that the u(t) signal can be adjusted flexibly to produce the optimal PWM values. The PWM pulses of the NSMC method can be obtained as follows

$$\text{PWM} = \begin{cases} 1, \text{ when } u(t) \ge \text{nlevel}(L_x + 0.5) \\ 0, \text{ else} \end{cases} \tag{9}$$

Fig. 4 presents a comparison of PWM pulses between the conventional POD modulation method and the NSMC modulation method. The switching frequency of IGBTs during a control signal cycle of 0.02 s is illustrated in Fig. 4(a) and 4(b) for the conventional POD and NSMC, respectively. As depicted, the switching number of IGBTs in the NSMC method is 29, whereas, in the conventional POD method, it is 51. This comparison demonstrates that the proposed NSMC method is capable of reducing the switching frequency of IGBTs, leading to improved lifetime and lower switching loss.

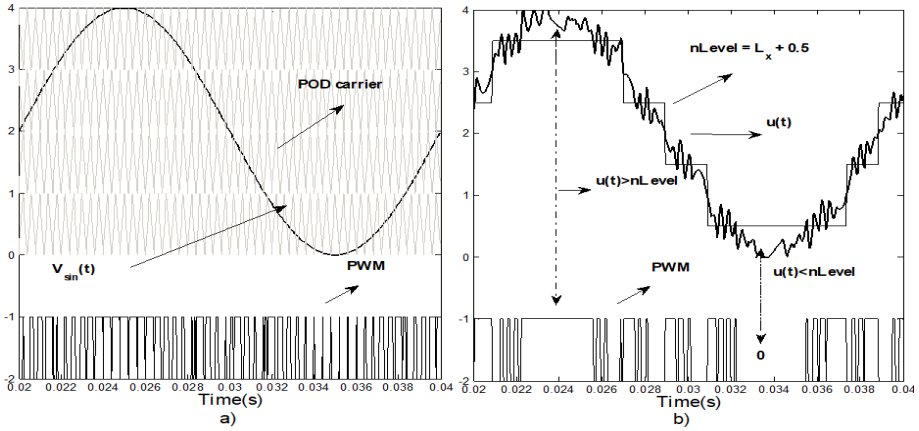


Fig. 4 - Generate PWM pulses (a) POD method; (b) NSMC method

The comparison results of $\sum S_{xjj}$ under the POD modulation method and NSMC method are shown in Fig. 5. As can be seen, the value of L_{min} = 5 and L_{max} = 7 under the survey time of 0.02 s can be determined with n = 5. Clearly, the

$\sum S_{xjj}$ of the NSMC method is less than the POD modulation method. Therefore, with the proposed NSMC method, the condition for reducing the CM voltage is satisfactorily met.

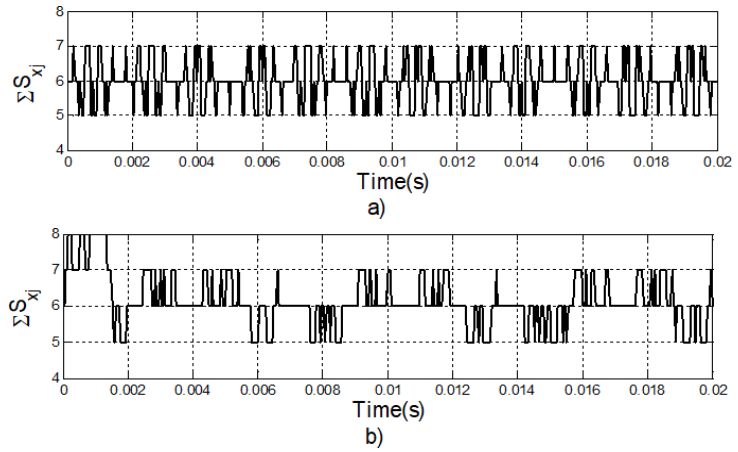


Fig. 5 - ∑Sxj value (a) POD method; (b) NSMC method

3. Design of Controller

This section develops a robust control method based on the proposed NSMC method to produce the control signal u(t), as discussed in the previous sections. The control law of the new controller is enhanced to eliminate the chattering that results from the high-frequency switching law around the sliding-mode surface. Additionally, the newly designed controller improves convergence speed and ensures the robustness of the controller. The following section provides details of the design for the new controller.

3.1 First-Order Low-Pass Filter

The purpose of designing LPF is to enhance stability and minimize oscillation that can arise from sudden and significant fluctuations in the load current. The frequency response and phase shift are graphically represented in Fig. 6. At cut-off frequency f_c, the output amplitude of the filter is reduced -3dB and has a phase delay -45°. The signal with frequency is greater than f_c, which will decline rapidly with the slope -20dB/decade. The transfer function for the LPF is given by

$$H(s) = \frac{1}{1+\tau s}, \quad \tau > 0 \tag{10}$$

where r is the time constant, and s is the Laplace variable.
The cut-off frequency of the filter can be determined as follows

$$f_c = \frac{1}{2\pi\tau} \tag{11}$$

The phase shift of the filter can be defined by

$$\varphi_c = -\arctan(2\pi f_c \tau) \tag{12}$$

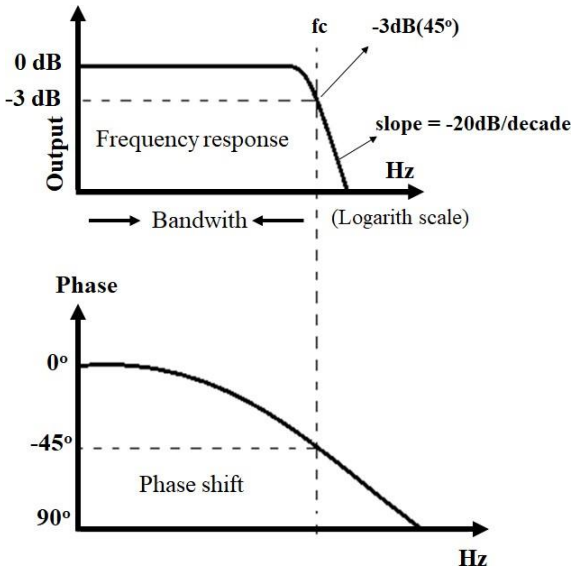


Fig. 6 - Frequency response and phase shift of a first-order low-pass filter

3.2 Proposed NSMC Controller

The system state will reach the sliding-mode surface from far away and slide along the sliding surface in the manifold s = 0. The phase trajectory of the system will be approached above or below the sliding-mode surface. This behavior leads to chattering phenomena and poses a system performance drawback. To address this issue, this research employs the tansig function with a continuous signal and the integral sliding-mode surface to guarantee an optimal phase trajectory. The state-space trajectories, illustrating the effectiveness of this design approach, are depicted in Fig. 7. From the robust control model for the CHB-5LI in Fig. 2 and considering the equation (10), the output of the controller can be established as

$$u_s(t) = (\tau s + 1)u(t) = \tau\dot{u}(t) + u(t) \tag{13}$$

Substituting (1) into (13), the following equation can be obtained as

$$u_s(t) = \tau\left(L\ddot{i}_x(t) + R\dot{i}_x(t)\right) + L\dot{i}_x(t) + Ri_x(t) \tag{14}$$

Equation (14) can be rewritten as follows

$$\ddot{i}_x(t) = \frac{1}{\tau L}\left(u_s(t) - \tau R\dot{i}_x(t) - L\dot{i}_x(t) - Ri_x(t)\right) \tag{15}$$

Due to the second-order function, the sliding-mode surface with $c_1 > 0$ should be chosen to satisfy the Hurwitz stability condition. The integral sliding-mode surface is given by

$$S(t) = c_1 e(t) + \dot{e}(t) \tag{16}$$

where error can be defined as $e(t) = c_2 i_x^*(t) - i_x(t)$; $i_x^*(t)$ is the reference current; $i_x(t)$ is the feedback current; c_2 is the constant, which is suggested to be added to reduce the steady-state error of the output value of inverter. Taking the derivatives on both sides of the sliding-mode surface (16), the following equation can be obtained as follows

$$\dot{S}(t) = c_1\dot{e}(t) + \ddot{e}(t) = c_1\dot{e}(t) + (c_2\ddot{i}^*(t) - \ddot{i}_x(t)) \tag{17}$$

Substituting (15) into (17) yields

$$\dot{S}(t) = c_1\dot{e}(t) + c_2\ddot{i}_x^*(t) - \frac{1}{\tau L}\left(u_s(t) - \tau R\dot{i}_x(t) - L\dot{i}_x(t) - Ri_x(t)\right) \tag{18}$$

The positive Lyapunov function is selected as

$$L = \frac{1}{2}S^2 \text{ and } \dot{L} = S\dot{S} \tag{19}$$

According to the Lyapunov stability criterion, $\dot{L}$ is necessary to determine the negative. Thus,

$$\dot{S}(t) = -\varepsilon\,\text{tansig}(S/\delta) - kS + \frac{R}{\tau L} i_x(t) + c_2 \ddot{i}_x^*(t) \tag{20}$$

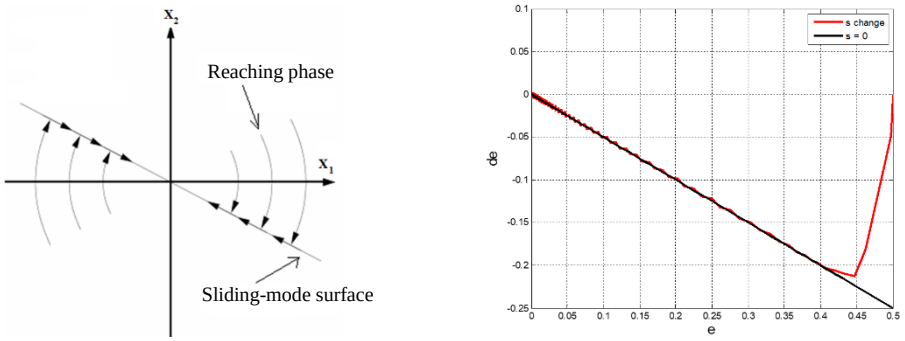
$$\text{and } y = \text{tansig}(S/\delta) = \frac{2}{(1 + e^{-2(S/\delta)})} - 1 \tag{21}$$

where constant $\delta > 0$; tansig is a continuous function, which is shown in Fig. 8; and ε is a positive constant and satisfies the condition in (22)

$$\varepsilon > \left| \frac{R}{\tau L} i_x(t) + c_2 \ddot{i}_x^*(t) \right| \tag{22}$$

Substituting (20) into (19) yields

$$S\dot{S} = S\left(-\varepsilon\,\text{tansig}(S/\delta) - kS + \frac{R}{\tau L} i_x(t) + c_2 \ddot{i}_x^*(t)\right) = -\varepsilon(|S/\delta|) - kS^2 + S\left(\frac{R}{\tau L} i_x(t) + c_2 \ddot{i}_x^*(t)\right) < -\varepsilon|S/\delta| < 0 \tag{23}$$



(a) (b)

Fig. 7 - Space trajectories of sliding mode control (a) reaching phase; (b) phase trajectory

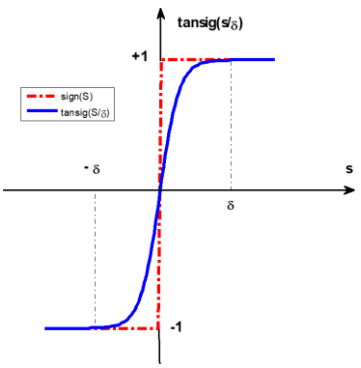


Fig. 8 - The comparison between sgn(S) and tansig(S/δ) function

As can be seen in (23), $S\dot{S} < 0$, and the designed control system satisfies the stable requirement according to the Lyapunov function.
From (20) and (18), equation (24) can be obtained as follows

$$- \varepsilon \text{tansig}(S/\delta\delta) - kS = c\ \dot{e}(t) - \frac{1}{\phi u\ (t) - \tau R\dot{i}\ (t) - L\dot{i}\ (t)\phi} \quad (24)$$

Finally, the robust sliding-mode control law without carrier wave for the multi-level inverter can be established as

$$u_S(t) = \tau L\left[c_1\dot{e}(t)+\varepsilon\,\text{tansig}(S/\delta)+kS+\frac{R}{L}\dot{i}_X(t)+\frac{1}{\tau}L\dot{i}_X(t)\right] \quad (25)$$

4. Simulation and Experimental Verification

In order to demonstrate the effectiveness of the proposed NSMC method, simulation and experimental tests are conducted on the same CHB-5LI with R-L load. Conventional POD modulation was utilized for comparison purposes to provide a fair evaluation. The accuracy of the results was verified using the MATLAB/Simulink environment. The current reference values are set at 1.5 and 2.5 A, respectively. The parameters used in both the simulation and experiment are listed in Table 2. A diagram of the NSMC method applied to the CHB-5LI with R-L load is illustrated in Fig. 9.

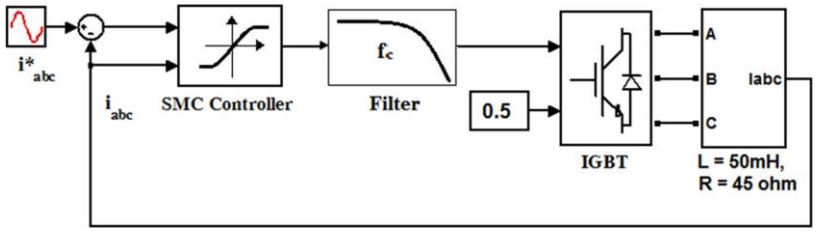


Fig. 9 - The simulation diagram

Table 2 - Test parameters

	Parameters	Symbol	Values
Inverter	Inductor L	L	50 mH
	Resistor R	R	45 Ω
	Sampling time	T_s	40 µs
	Switching frequency	f_c	2.5 kHz
	Deadtime		2.5 µs
	DC voltage	V_{dc}	60 V
Controller	Constant gain	c_1	3
	Constant gain	ε	1000
	Constant gain	σ	1.2
	Constant gain	c_2	1.09

4.1 Simulation Verification

Fig. 10 presents the simulation results of line-line voltage (V_{ab}), phase a current (i_a) and CM voltage (V_{cm}). It can be seen that the proposed NSMC method achieves steady-state within a mere 0.002 s. This result confirms that the NSMC method can guarantee rapid convergence in a short period, indicating its effectiveness.

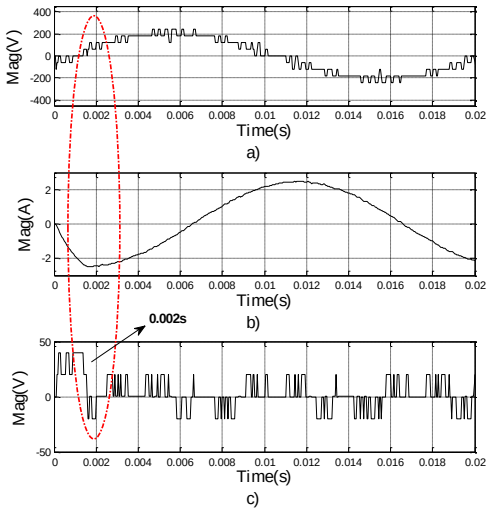


Fig. 10 - The voltage and current waveform. (a) voltage V_{ab};(b) phase a current (I_a); (c) voltage V_{cm}

Fig. 11 to 14 show the comparison results between the NSMC method and the conventional POD modulation. Two cases were considered with the reference current values of 1.5A and 2.5A. The total harmonic distortion (THD) for the line-to-line voltage and current of phase a were analyzed using fast Fourier transform (FFT) analysis. The phase voltage (V_{an}), line-to-line voltage (V_{ab}), THD V_{ab}, CM voltage (V_{cm}), current of phase a (i_a), and THD i_a were evaluated according to the quality standards. The feedback current for both the NSMC and conventional POD methods accurately tracked the reference current in both cases. However, the NSMC method had better quality than the conventional POD method. In the case of reference current 1.5A, as seen in Figs. 11 and 12, the THD V_{ab} values of the NSMC and conventional POD are 29.22% and 38.45%, respectively. Additionally, the THD i_a values are 1.98% and 2.56% for the NSMC and the conventional POD method, respectively.

The results depicted in Figs. 13 and 14 reveal that when the reference current is augmented from 1.5 to 2.5A, the THD i_a and THD V_{ab} under the NSMC method consistently demonstrate smaller values than the conventional POD method. Specifically, in the case of THD i_a, the NSMC method presents a reduction of 1.28% compared to the value of 1.34% exhibited by the conventional POD method. Similarly, THD V_{ab} manifests at 21.96% and 24.12% for the NSMC and conventional POD methods, respectively. The comparison outcomes of the FFT analysis are presented in Fig. 15.

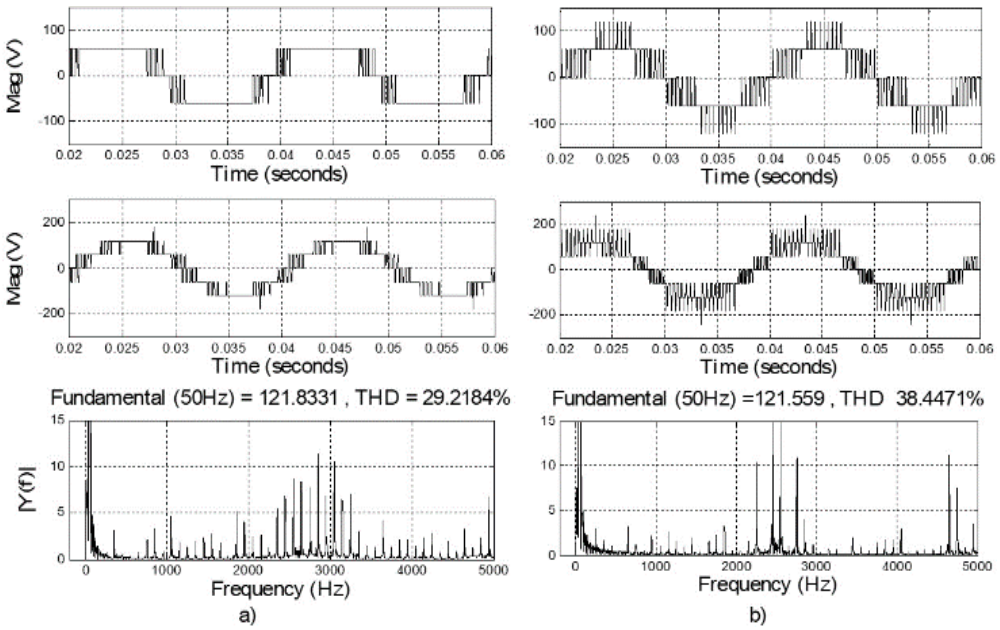


Fig. 11 - Simulation results of V_{an}, V_{ab}, THD V_{ab} with i^*_{abc} 1.5A (a) NSMC method; (b) POD method

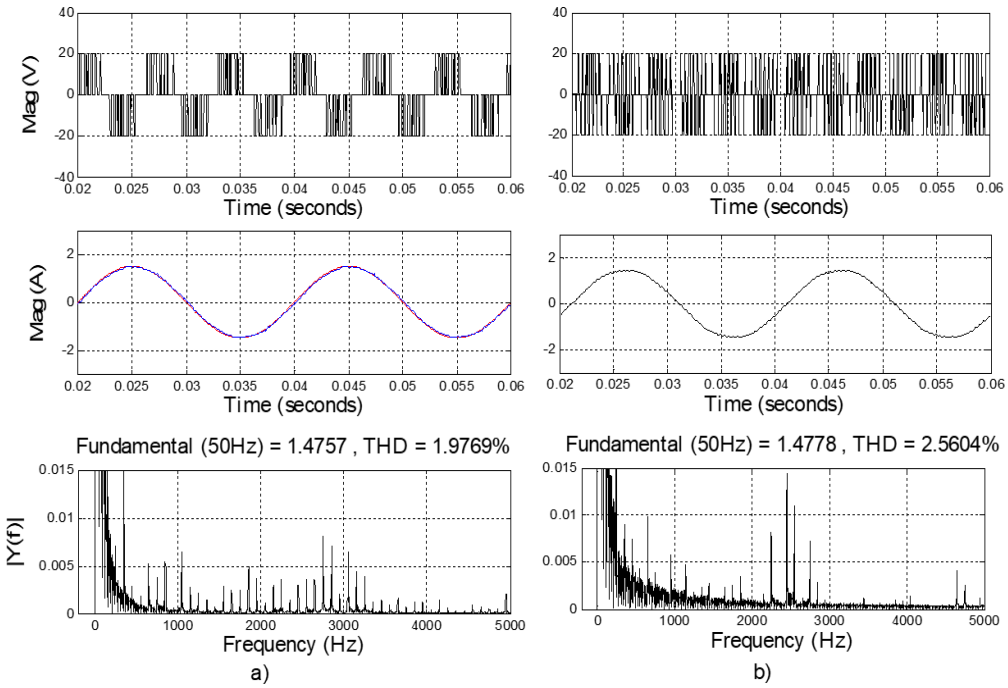


Fig. 12 - Simulation results of V_{cm}, i_a, and THD i_a with i^*_{abc} 1.5A (a) NSMC method; (b) POD method

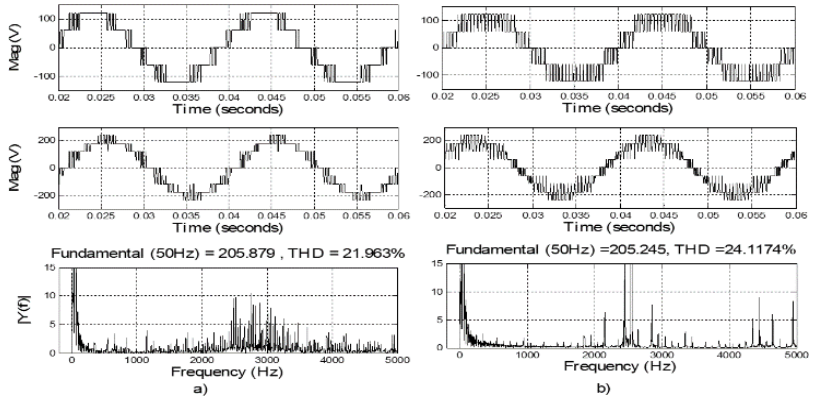


Fig. 13 - Simulation results of V_{an}, V_{ab}, THD V_{ab} with i^*_{abc} 2.5A (a) NSMC method; (b) POD method

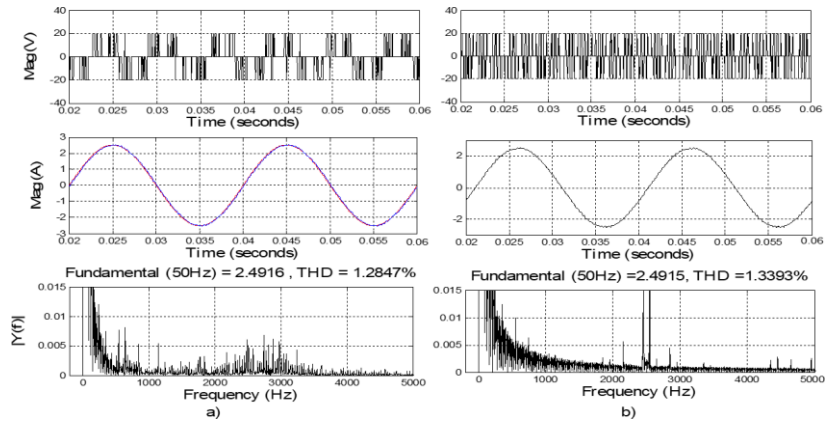


Fig. 14 - Simulation results of V_{cm}, i_a, and THD i_a with i^*_{abc} 2.5A (a) NSMC method; (b) POD method

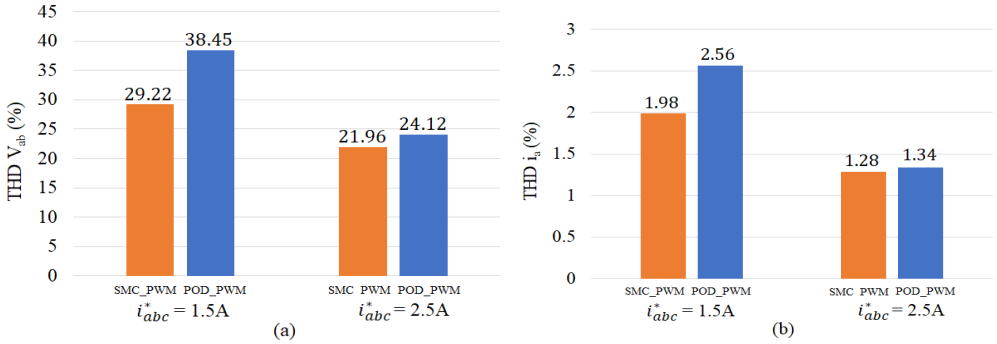


Fig. 15 - Comparison results of FFT analysis

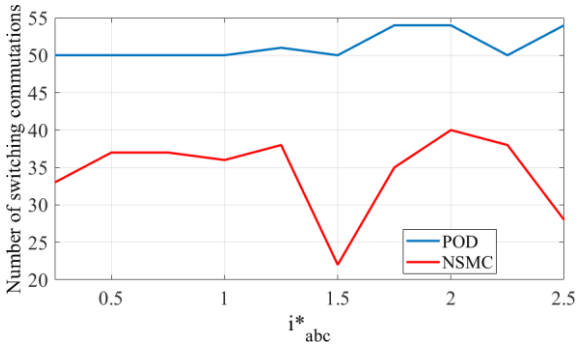


Fig. 16 - Comparison of the number of switching commutations in a cycle of the control signal

The simulation results confirm that the measured current value always accurately follows the reference current value. Moreover, the proposed NSMC method consistently produces a superior output for the inverter with lower CM voltage and less total harmonic distortion percentage than the conventional POD method. Additionally, it is apparent from Fig. 16 that the NSMC method requires fewer switching commutations than the conventional POD method.

4.2 Experimental Verification

In order to guarantee the accuracy of the simulation results, experiments are conducted on a real CHB-5LI platform. The experiment hardware configuration can be found in Fig. 17. The NSMC method algorithm is developed on MATLAB/Simulink and then integrated into the DSP TMS320F28379. The ADC block analyzes both the reference current ï* and the feedback current i_{abc}.

Fig. 17 - Setup of experiments

The experimental results of the NSMC and conventional POD methods with a reference current of i^* = 1.5A are presented in Figs. 18 and 19. The Fig.s show that the NSMC method outperforms the conventional POD method in terms of robustness and quality. Specifically, the THD V_{ab} and THD i_a of the NSMC method, as shown in Fig. 18 and Fig. 19, are 53.25% and 2.9%, respectively, while the conventional POD method has higher THD values of 61.18% and3.59% for THD V_{ab} and THD i_a, respectively. Furthermore, the CM voltage of the NSMC method is superior to that of the conventional POD method. The results of the CM voltage with the reference current of 1.5A for the two methods are displayed in Fig. 19.

Once again, it has been shown that the NSMC produces exceptional results in terms of quality and performance when a reference current of 2.5A is utilized, similar to the findings with a reference current of 1.5A. This comparison is depicted in Figs. 20 and 21. Furthermore, the FFT analysis performance metric is illustrated in Fig. 22, which confirms a strong correlation between the simulation and experimental results. These results validate the efficacy of the proposed NSMC method for CHB-5LI.

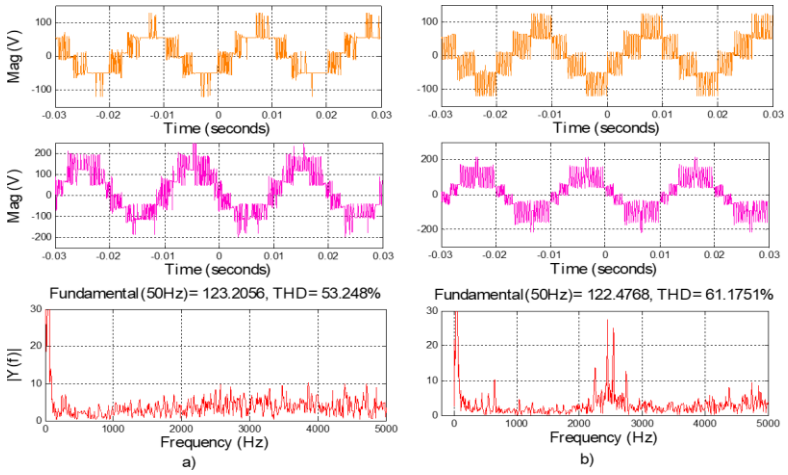


Fig. 18 - Experimental results of V_{an}, V_{ab}, THD V_{ab} with i^*_{abc} 1.5A (a) NSMC method; (b) POD method

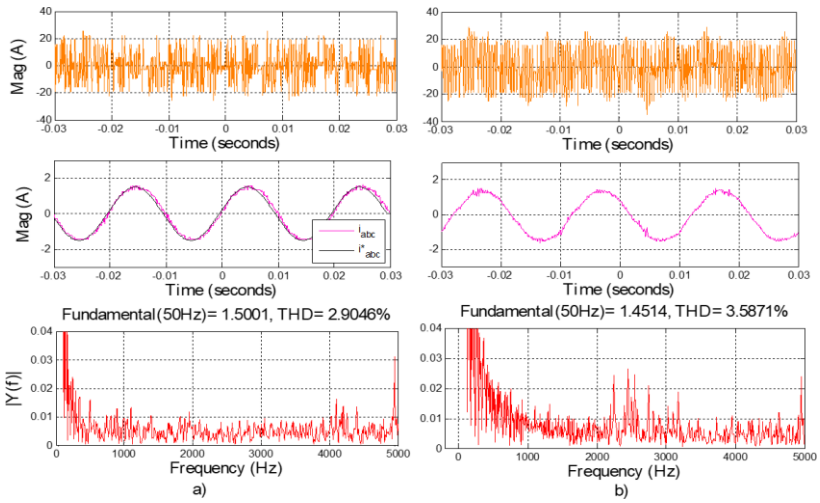


Fig. 19 - Experimental results of V_{cm}, i_a, and THD i_a with i^*_{abc} 1.5A (a) NSMC method; (b) POD method

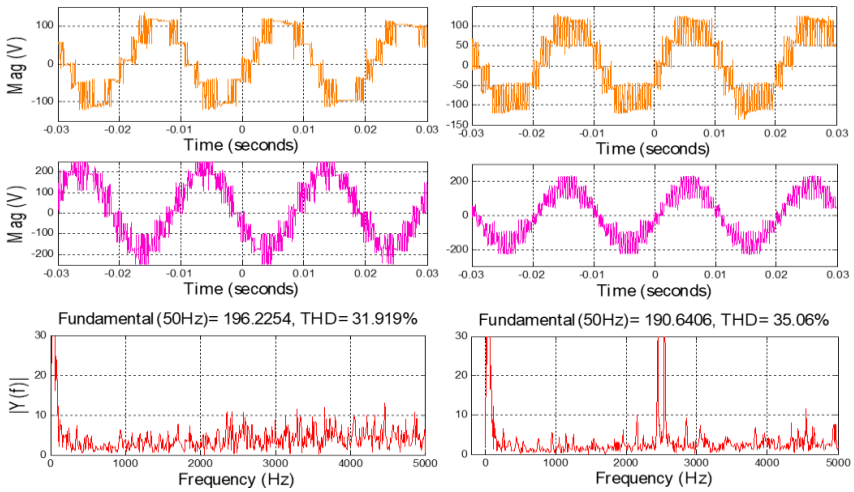


Fig. 20 - Experimental results of V_{an}, V_{ab}, THD V_{ab} with i^*_{abc} 2.5A (a) NSMC method; (b) POD method

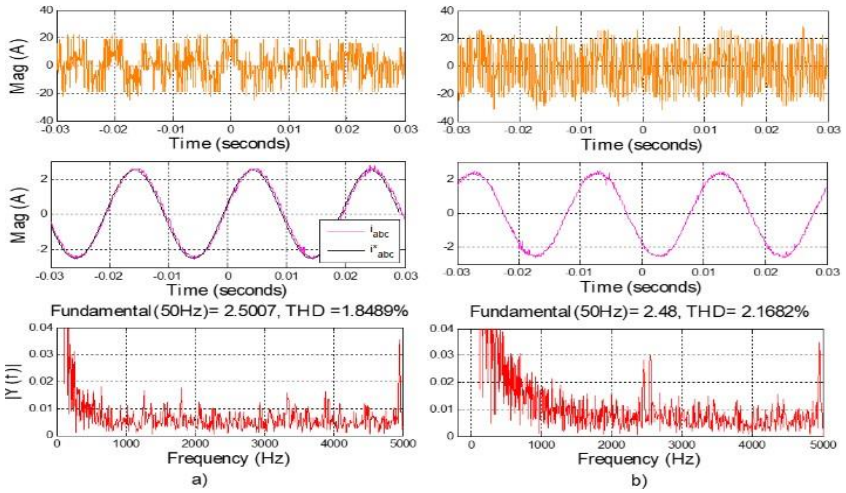


Fig. 21 - Experimental results of V_{cm}, i_a, and THD i_a with i^*_{abc} 2.5A (a) NSMC method; (b) POD method

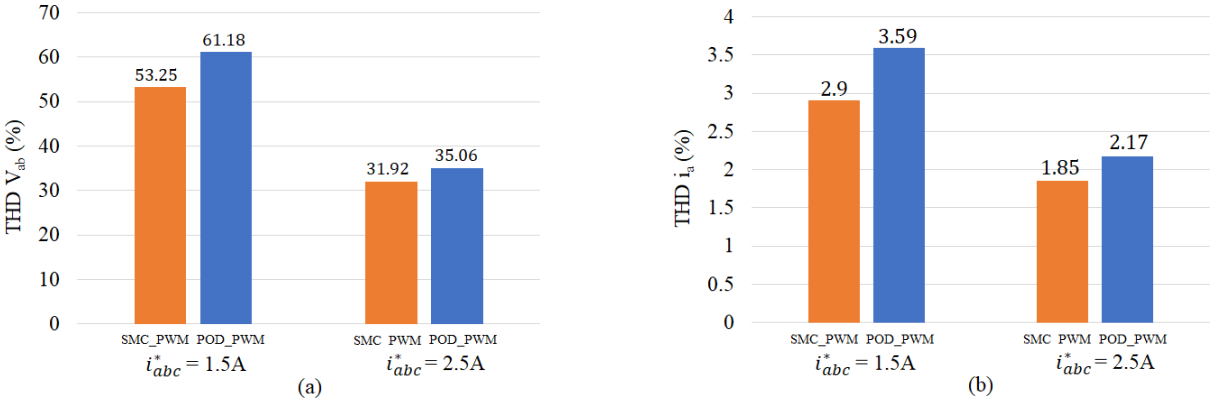


Fig. 22 - Experimental comparison results of FFT analysis with two methods

5. Conclusion

This article introduces a new robust control method for the CHB-MLIs based on the NSMC. Unlike traditional methods, this approach improves the output quality of the inverter, reduces CM voltage with high-order harmonics, and achieves stable and sustainable control without utilizing carrier wave techniques to modulate the PWM pulses. The NSMC method modulates the PWM pulses by comparing the control signal u(t) from the output signal of the NSMC

controller and the comparator levels. To address the chattering problem around the sliding-mode surface and increase convergence speed, the design of the control system utilizes a nonlinear integral sliding-mode surface integrated with a continuous control law. The LPF is also proposed to enhance stability and reduce oscillation resulting from quick and significant changes in the load current amplitude. The stability of the control system is verified using Lyapunov criteria. To demonstrate the effectiveness and superiority of the NSMC method, a comparison between the proposed method and the traditional carrier wave-based PWM technique known as POD is conducted through simulations and experiments using a CHB-5LI with an R-L load. The results show that the NSMC method achieves strong robustness and high performance for CHB-MLI control systems. The proposed method consistently produces better output quality for the inverter, with significantly reduced CM voltage, fewer high-order harmonics, and lower switching frequency with less loss. Therefore, the NSMC method proposed has been demonstrated to ensure stable and robust control for CHB-MLIs.

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