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IJIE

Journal homepage: http://penerbit.uthm.edu.my/ojs/index.php/ijie
ISSN : 2229-838X e-ISSN : 2600-7916

The International Journal of Integrated Engineering

Temperature Variation Operation of Mixed-V_T 3T GC-eDRAM for Low Power Applications in 2Kbit Memory Array

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DOI: https://doi.org/10.30880/ijie.2022.14.03.021
Received 30 November 2021; Accepted 07 June 2022; Available online 20 June 2022

Abstract: Embedded memories were once utilized to transfer information between the CPU and the main memory. The cache storage in most traditional computers was static-random-access-memory (SRAM). Other memory technologies, such as embedded dynamic random-access memory (eDRAM) and spin-transfer-torque random-access memory (STT-RAM), have also been used to store cache data. The SRAM, on the other hand, has a low density and severe leakage issues, and the STT-RAM has high latency and energy consumption when writing. The gain-cell eDRAM (GC-eDRAM), which has a higher density, lower leakage, logic compatibility, and is appropriate for two-port operations, is an attractive option. To speed up data retrieval from the main memory, future processors will require larger and faster-embedded memories. Area overhead, power overhead, and speed performance are all issues with the existing architecture. A unique mixed-V T 3T GC-eDRAM architecture is suggested in this paper to improve data retention times (DRT) and performance for better energy efficiency in embedded memories. The GC-eDRAM is simulated using a standard complementary-metal-oxide-semiconductor (CMOS) with a 130nm technology node transistor. The performance of a 2kbit mixed-VT 3T GC-eDRAM array were evaluated through corner process simulations. Each memory block is designed and simulated using Mentor Graphics Software. The array, which is based on the suggested bit-cell, has been successfully operated at 400 MHz under a 1V supply and takes up almost 60-75% less space than 6T SRAM using the same technology. When compared to the existing 6T and 4T ULP SRAMs (others' work in K. Sharma et al.and A. Goyal et al.) the retention power of the proposed GC-eDRAM is around 80-90% lower.

Keywords: GC-DRAM, embedded memories, DRT, leakage

1. Introduction

Moore's law is facing a great challenge as further downscaling of electronic devices became at the cost of performance, further shrinking of electronic devices is likely to cause device imperfection due to manufacturing process. VLSI systems-on-chip (SoCs) implemented in aggressively scaled CMOS technologies are characterized by high leakage currents. The drawbacks of different types of RAMs are further enhanced at scaled technologies, where increased subthreshold leakage currents (I_{SUB}) and decreased in-cell storage capacitances caused a faster data deterioration in case of GC-eDRAM, while despite the several advantages of SRAM as it's fast access speed, being robust and having a static data retention, failure rates are recorded under voltage scaling. So, in the context of those emerging challenges working

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on solutions to minimize the size consumed by memory and increase its performance will help in prolonging Moore's law [1] and producing processors that can adapt to the vast increase in applications [2].

In embedded memories and VLSI SoCs, memory designs were targeting several applications as smartphones, tablets, servers, laptops in addition to biomedical implants and communication systems [3]. Those embedded memories often used to relay between the central processing unit (CPU) and the main memory [4]. From quality design perspective, it's more advantageous to embed a larger memory directly within the chip, instead of relying on external memory, as using an external memory will feature capacitive lines [5] and will mostly end up by giving a lower performance in terms of speed and power consumption.

Currently, embedded memories take around 50% of the power and area of VLSI SoCs [6]. Fig. 1 shows the contribution of static random-access memory (SRAM) in the layout area of a high-end 45 nm intel core i7 processor.

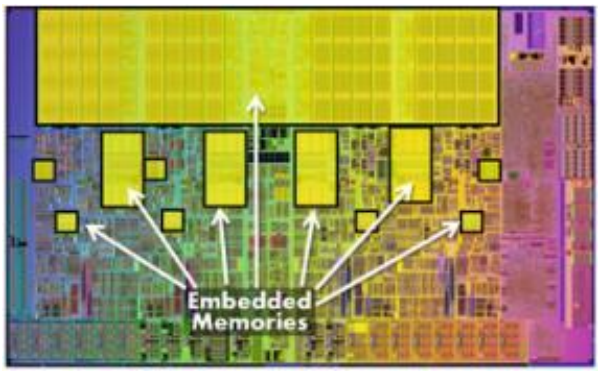

Fig. 1 - layout of 45 nm Intel core i7 processor [7]

Furthermore, embedded memories are one of the main consumers of power in most VLSI SoCs [8]. For instance, the power consumption of embedded memories for an ultra-low-power specific processor called TamaRISC-CS was found to be ranging from 70% to 95% of the total power [9]. In addition to this, it was found that the total dynamic and static power consumed by chips for motionless applications is up to 100w [6], while it was stated by ITRS in 2009 that for portable applications the total power consumption for the VLSI SoC processors should not exceed 0.5w or 2w for consumer processors as tablets. At the same time Fig. 2 shows that the power consumption of embedded memories will reach almost half of the total power consumed by the processors in the upcoming 15 years, this made reducing power consumption one of the most important aspects in embedded memory designs [10], as this will guarantee the near to ideal functionality of the processors for several years which is a key requirement in some applications as implanted biomedical devices [11].

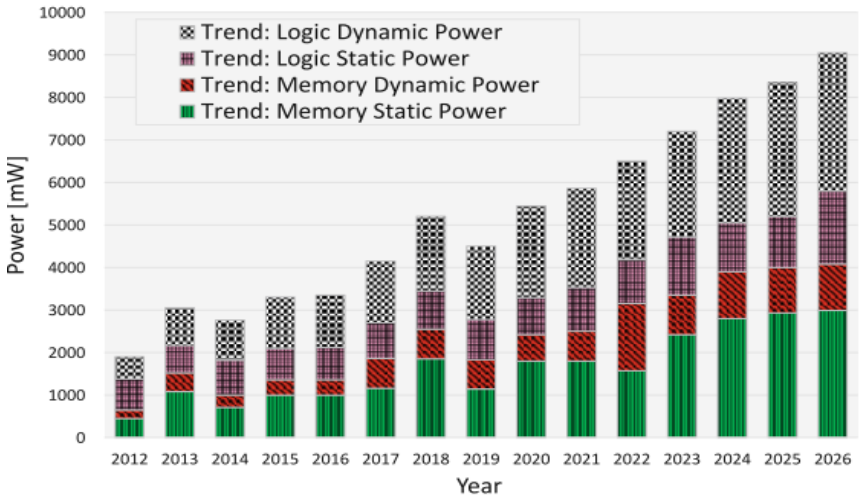

Fig. 2 - Expected breakdowns of power for portable consumer electronics [6]

This paper focuses on GC-eDRAM as an alternative for standard embedded memory designs. GC-eDRAM offers a topology that is different from DRAM, DRAM require a capacitor, while GC-eDRAM does not require a capacitor, in which it does not require any complicated or special steps for the process of manufacturing; this makes it fully compatible with the current standard CMOS technology and comparable to SRAM. Active elements are used to incorporate the read port of the cell, which is the basic storage unit; In fact, GC-eDRAMs are usually supplied with dual-port operations as

GCs have separate write and read ports. This gives GC-eDRAMs an additional advantage as multiple read and writes can be done without adding extra transistors. In this context a proposed GC-eDRAM was designed and evaluated in 130nm CMOS technology. The cell was evaluated separately to confirm it's integrability and then in a memory array to evaluate its performance in terms of DRT, leakage power and area. Post layout simulations were done including all the memory blocks (read and write decoders, buffers, level-shifter, drivers, pre-charge circuit and sensing amplifiers). The proposed cell showed a high decrease in retention power which was found to be 80-90% lower than the power consumed by SRAM cells in the same technology presented in this work [12]. The maximum operating frequency reached 250 MHz at typical process corner while it reached 400 MHz at fast process corner. The worst-case DRT was measured to be 2.8uS at 85℃ which is acceptable as we preferred in our design to have a high speed with a moderate DRT. The paper is divided into five more sections, in the second section the method of operation of GC-eDRAM and why its topology is hard to estimate will be discussed, in the third section the methodology in which the proposed cell was chosen will be explained. In the fourth section a brief about each of the memory blocks will be given and explained. In the fifth section the results of the simulation will be discussed and compared to different topologies. At last, the paper will be concluded.

2. GC-eDRAM

The GC-eDRAM consists of three main parts, the storage node mainly from the parasitic gate capacitance (SN), the read port, and the write port. GCs include a write word line (WWL), a read bit line (RBL), and a read word line (RWL), which makes it suitable for two port operations. The cell can be triggered into three operation modes: hold mode in which no read or write operations are performed, the read mode, and the write mode. During the hold mode, degradation of the SN will result in a degraded one in case of NMOS cell and a weak zero in case of a PMOS cell.

2.1 Method of Operation

As shown in Fig. 3, data is stored in each cell in the form of a charge on the storage node (SN) formed by the read transistor (MR) gate capacitance and parasitic capacitance junction/wire. The selected GC's write transistor (MW) is discharged during a write operation to transfer the new data level from the write bit line (WBL) to the SN, then an underdrive negative voltage is applied to the selected write word line (WWL) to allow the transfer of a clean logic ' 0 ' in case of PMOS MW, while an overdrive positive voltage is applied in case of NMOS MW. In case of PMOS read Transistor (MR), all read bit lines (RBLs) are discharged to the ground to start a read operation. Then, the read word line (RWL) is charged to V_{DD}, If a GC stores ' 1 ' reasoning, the MR will remain off and the associated RBL will stay at a level of '0'. If the GC stores a ' 0 ' logic, though, the RBL may start charging through the MR. The sensing amplifiers then will sense the current in order to give the reading at the selected cell. Exactly the opposite process is applied in case of a read from an NMOS transistor. During hold state GC-eDRAMs are characterized by the dynamic property in which the stored data will degrade as time passes because of the leakage currents [13], that's why they require refresh cycles in order to remain the data unaffected.

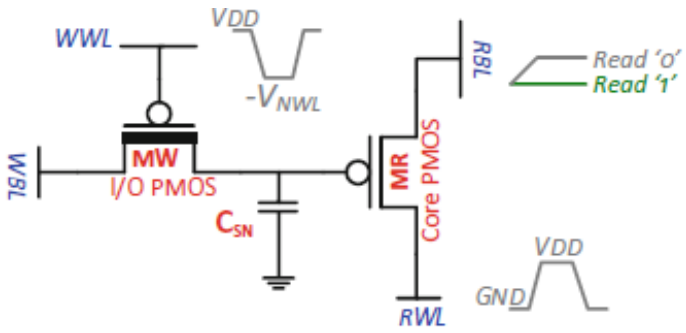

Fig. 3 - 2T PMOS waveforms for write/read access [14]

2.2 Available Topologies

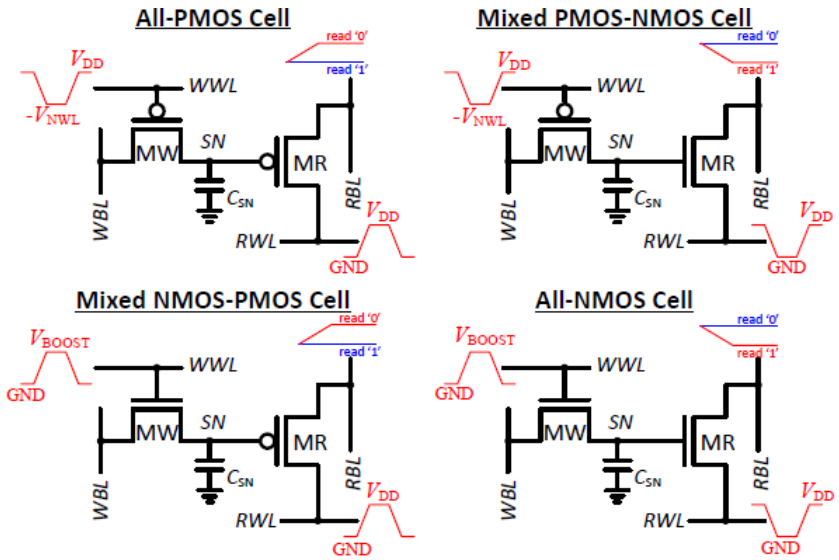

Fig. 4 - Different implementations for 2T GC-eDRAM [15]

Gain-cell cell topologies included many varieties as 1T1C, 2T, and 3T with an optional diode [8] or 4T [16] and 5T [17] with a feedback mechanism. Fig. 4 shows a 2T GC-eDRAM using different combinations as all PMOS cell, Mixed PMOS-NMOS cell, all NMOS cell and mixed NMOS-PMOS cell.

Implementing designs for GC-eDRAM cells cannot only be achieved by varying the number of NMOS and PMOS inside the cell, but also by varying the types of MOSFETs used between core and I/O devices [18], different combinations following those two methods gives a great range in variability for the designed cell and accordingly in the resulted leakage currents, DRTs, maximum frequency, read/write access speed, availability of memory array [19] in addition to various area and power overheads. Increasing performance was also targeted by modelling and characterization of new sub-V_T GC-eDRAMs in order to get the lowest leakage current [20] and optimum threshold by optimizing several parameters as subthreshold slope (SL), DIBL and I_{on}/I_{off} ratio.

Cells were also implemented to achieve different techniques for tolerating soft errors or single event upsets (SEUs) using both architectural and circuit techniques [21], an example of that is by duplicating the standard 2T cell into the four-transistor structure in which the cell will have two storing nodes to be compared, other examples are using parallel sensing schemes [22] in order to sense the inverting of storing nodes and different switching thresholds, using body biasing [23] in order to improve DRT, using dual read out functionality to detect errors or using replica scheme in order to evaluate the performance of the fabricated chip and detect the optimum refresh cycles frequency instead of assuming worst case condition which usually result in consuming more power.

2.3 Proposed Cell

A 4T GC was not proposed because it is more suitable for sub-100nm technology in order to increase the DRT of the cell, whereas in above-100nm technology, 2T and 3T GCs offer a reduced area and an accepted DRT of microseconds or milliseconds. The maximum frequency of a 4T GC is also slightly lower than that of a 3T GC because the 4T consumes larger areas, resulting in longer RBLs and, consequently, a longer read access time (RAT). 3T GC and 2T GC have approximately 20% and 35% less area than 4T GC, respectively [9].

So, in order to ensure a high-density memory, a choice can be made between the 3T and 2T GCs. However, a 3T GC will be used to avoid the RBL saturation issue and provide a faster RAT. At the GC design stage, the NMOS body terminals will be shortened together and connected across all the GCs in the memory array to provide controllability over the threshold voltage, which will aid in optimizing the DRT, availability, and maximum frequency of the memory for the required application. Two low-threshold voltage transistors will be used as read transistors because they will result in a low RAT [4]. For the write port, a high threshold NMOS transistor will be used to provide fast write access with low leakage current.

The proposed cell design for this work is shown in Fig. 5; the width of the write transistor was doubled to allow for fast transmission of '0' or '1' to the storage node. To perform body biasing for further testing and development of the project, an input pin V_{BB} was added. The 3T GC and memory array will only be tested at zero body biasing (BB) for the time being.

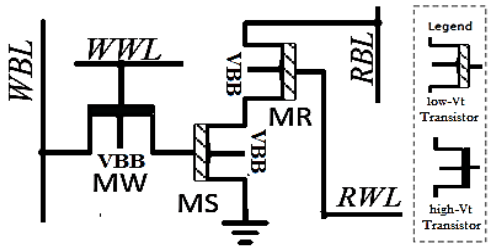

Fig. 5 - Proposed mixed-V_T 3T GC-eDRAM

3. Memory Array Blocks

In order to be able to test the proposed GC-eDRAM cell, several additional blocks are required for the implementation of the memory array. These main blocks are the write and read address decoders (note that this memory array requires two decoders for read and write as it supports two port operation), pre-charge circuit, a pre-WWL driver followed by the driver circuit, a level-shifter, and data buffers.

Address decoder is an essential part of the memory architecture, in which it should respond effectively at high frequency. Decoder design largely affects the RAT, write access time (WAT), and power dissipation. The decoder's function is to decode a given input address and to enable a particular input for the pre-WWL driver. Two main considerations should be taken into account while choosing the decoder circuit, which is a good circuit technique and the transistor sizing. Various types of decoders are available in literature such as static decoders and dynamic decoders, and each of the two types can be implemented using NAND and NOR gates in addition to inverters. For conventional static decoders, in NOR decoders all the outputs of the array will be low by default, with the exception of the selected row, which is high while in case of NAND decoders, the opposite occurs and since the interface between decoder and memory often includes a buffer, it can be made inverting. Conventional decoders occupy more space, feature lower speed, and consume more power. Decoders can also be implemented using mixed logic design methods by combining the pass transistor logic, transmission gate logic, and complementary metal-oxide-semiconductor (CMOS) technology in order to provide the desired performance [24]. NAND dynamic decoder is characterized by less area and lower power than NOR decoder.

NOR array decoders [25] has several advantages over other types of decoders that's why it has been used in this work. It offers a smaller number of transistors, higher speed, the power consumption is less, where it can be controlled by varying the pulse of a CTL signal, which is connected to each pull up transistor of the circuit. The pulse width can be decided based on the required time to decode an address. Fig. 6 shows the circuit of a single 3:8 decoder. Nine 3:8 decoders will be combined to form a 6:64 decoder, which will be used as an address decoder in this project.

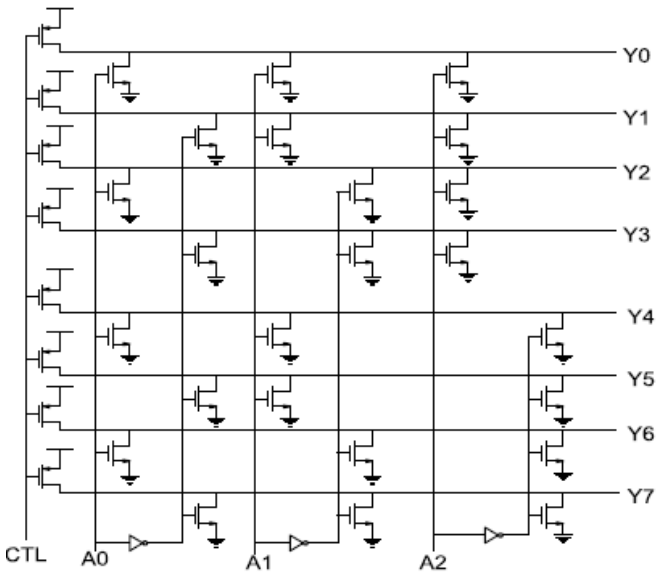

Fig. 6 - 3:8 dynamic NOR array decoder circuit [25]

Simply a PMOS pass transistor will be used as a pre-charge circuit, this will ensure a strong one and a fast evaluation for the RBL line by the sensing amplifier. A voltage-based differential sense amplifier with an external reference voltage (V_{ref}) presented in [18] will be used to enable faster evaluation of the RBL voltage.

For the write port, a pass transistor is typically used. As a result, when using an NMOS write transistor, a write '1' operation suffers from degradation. As a result, the voltage for the WWL should be boosted to enable a fast logic '1' write. In order to increase the voltage, a global conventional level-shifter which was presented in [18] will be used.

A pre-WWL driver will be used, followed by an inverter as a WWL driver, to drive the WWL of a specific row when it is triggered by the write decoder. Both drivers will use boosted voltage and will be composed of high threshold MOSFETs. Two inputs will go into the pre-WWL driver: the shifted output from the level-shifter connected to the pull-up PMOS transistor, and the other input from the AND gate that follows the decoder, this will give a greater control over the write cycle. The pre-WWL driver's output is connected to the WWL driver's input, which inverts the signal and sends it to the WWL for that row. When no write operation is performed, this method ensures that the boost voltage is isolated from the main source and will also result in lower leakage currents.

4. Results and Discussion

The memory design space is complicated due to the presence of many design variables that have a significant impact on memory capacity metrics. Because of the many bit-cell topologies and dynamic trade-offs, such as those between DRT and access time, the design room for GC-eDRAM is even greater than for SRAM. As a result, various designs of GC-eDRAM cells must be tested and evaluated in order to determine the effect of each parameter, such as transistor configuration and sizing, on the performance of the GC-eDRAM array.

A test bench was made for each memory block and each of the blocks were tested at high frequencies, especially the decoder, where the post-layout simulation showed that it operated efficiently at 1GHz. This approach was followed to make sure that the memory speed will not be limited by any of those blocks. For the level-shifter circuit, the post-layout simulation results showed a small glitch at the negative, it can be removed using more complex designs to achieve a better performance, but for this work we will use the conventional level-shifter because it will give a lower area overhead and it will be sufficient for testing the memory array.

The memory cell layout consumed an area of 2.842x3.845µm^2, which is 60% to 75% less than the area consumed by a 6T SRAM implemented in the same technology in [26]. The cell operated at a minimum supply voltage of 0.85V and 1.1V boost voltage, and an optimum supply voltage of 1V and 1.3V boost voltage. The simulation results were all obtained at the optimum voltage. The SN capacitance was found to be around 0.7fF, which is within the expected range for minimum sized device [27]. The cell had a worst-case RAT and WAT of 504pS and 463pS at 25°C, respectively, and 483pS and 496pS at 85°C. A lower RAT at higher temperatures indicates a decrease in RBL parasitic capacitance as temperature rises. To ensure a fast response, the worst-case RAT was measured from the time the clock triggers the read decoder until the time when the output of the sensing amplifier begins to rise while reading a stored '1'. The reference voltage for the sensing amplifier was set to a value ranging between 0.75V and 0.8V. While the worst-case WAT was measured from the time the write decoder's clock was triggered to the time a '1' was stored to the SN.

Table 1 shows the key-features of the proposed memory cell. The small difference between the RAT and WAT indicates a good performance as this will ensure that the operating frequency will not be limited by a slow read operation. The DRT was found to be approximately 46µS at 25℃ and 4.7µS for the worst case at 85℃. The retention power which is composed of both the static and refresh power of the proposed GC-eDRAM showed about 80-90% lower consumption than the static power of 6T and 4T ULP SRAMs, which were proposed in [28].

Table 1 – Key features of the proposed 3T GC-eDRAM

Parameters	Cell features at 25℃	
Write transistor	NMOS HVT	
Read transistors	2 PMOS LVT	
Supply voltage	0.85-1V	
V_{boost}	1.1-1.3V	
C_{SN}	0.7fF	
Temperature	@25℃	@85℃
WAT	463pS	496pS
RAT	504pS	483pS
Write delay	28pS	27pS
Read delay	160pS	109pS
DRT	46µS	4.7µS
Leakage power	1.8nW	7.3nW
Write access power	10pW	18pW
Read access power	53.5pW	548.3pW

In order to test and evaluate the proposed mixed-V_T 3T GC-eDRAM, a 2Kbit memory array layout was created. Fig.7 shows the layout of the memory array including all blocks. The memory was tested at zero BB with a supply voltage of 1V and a boost voltage of 1.3V. The cells had a worst-case RAT and WAT of 2.76nS and 1.3nS, respectively, at 25°C, and 2.8nS and 1.5nS at 85°C. The read delay was 1.25nS at 25°C and 1.3nS at 85°C, while the write delay was 212.6pS at 25°C and 181pS at 85°C. Fig. 8 – (a) shows the deterioration of a stored '1' at TT corner process from the storage node at different temperatures sweeping from 25℃ until 85℃. The DRT was found to be 82S at 25°C and 6.9S at 85°C under worst-case conditions, where all write bit lines were driven with the opposite level of the SN.

The memory was tested at different frequencies, and the maximum operating frequency was determined to be 250 MHz at the typical NMOS typical PMOS (TT) process corner and 400 MHz at the fast NMOS fast PMOS (FF) process corner. At the FF process corner, the DRT was also measured and found to be 17µS and 2.8µS at 25°C and 85°C respectively. Fig. 8 - (b) shows the faster deterioration of a stored '1' at the FF corner process compared to the TT corner process at different temperatures sweeping from 25℃ until 85℃.

Therefore by evaluating the frequency and the DRT at 25℃ the availability of the memory was found to be 99.6% and 99% at TT and FF processes respectively, while at 85℃ the availability decreased to 95% and 93.6% at TT and FF processes respectively. A near 95% worst case availability shows that the refreshment cycles can be hidden and that GC-eDRAM could satisfy the needs of embedded memory applications. Table 2 shows the comparison for the maximum frequency, DRT, and availability at the two different corner processes at 25℃ and 85℃.

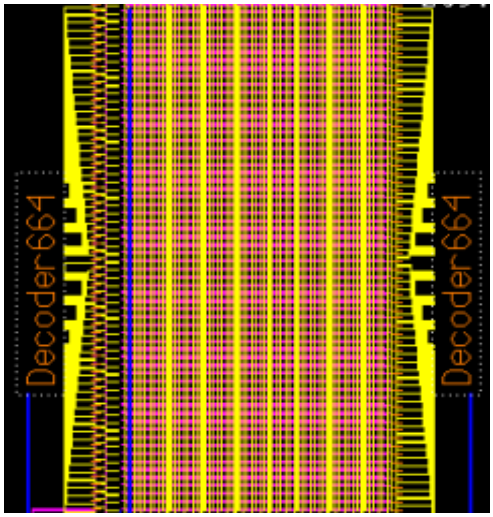

Fig. 7 – Memory array layout including all blocks

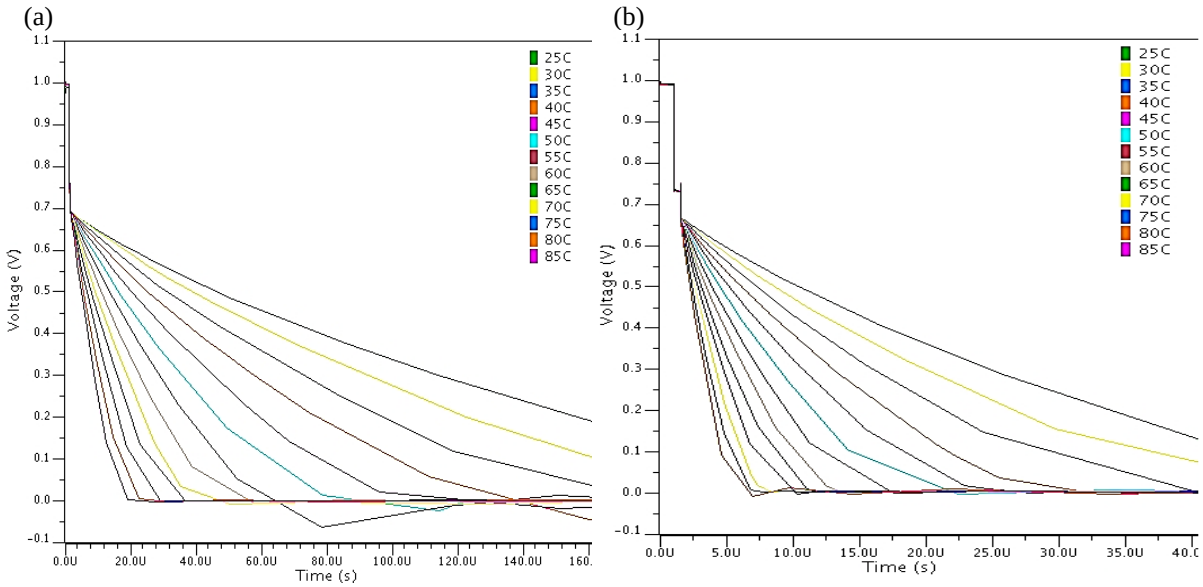

Fig. 8 – Temp. sweep analysis for the DRT of a 2Kbit mixed-V_T 3T GC-eDRAM array: (a) at TT corner process simulation; (b) at FF corner process simulation

Table 2 – Performance comparison in terms of frequency, DRT, and availability

Corner Process	f_{max} (MHz)		DRT (µS)		Availability (%)	
Temperature	@25℃	@85℃	@25℃	@85℃	@25℃	@85℃
TT	250	250	82	6.9	99.6	95
FF	400	400	17	2.8	99	93.6

A comparison between different topologies was carried out, but due to the lack of available literature for 130nm the comparisons were done against the 65nm topologies which are available in literature. Table 3 shows the comparison against asymmetric 2T GC [29], conventional 2T GC [30], and 3T Low-V_T GC [31]. The comparison shows that although the proposed cell was implemented in a larger technology, it was able to compete the frequencies of the other cells, but that was at the cost of the DRT. The memory array for the proposed cell was also able to operate at the lowest supply voltage.

Table 3 – Comparisons against other topologies in 65nm, all the cells were operating at 85℃

Parameters	Asymmetric 2T GC [29]	Conventional 2T GC [30]	3T Low-V_T GC[31]	Mixed-V_T 3T GC (This work)
Technology node	65nm	65nm	65nm	130nm
Supply voltage	1.2V	1.1V	1.2V	1V
Maximum array freq.	667MHz	250MHz	250MHz	400MHz
Retention time	110µs	10µs	5µs	2.8µS
Leakage power	N/A	N/A	N/A	7.3nW/bit

5. Conclusion

In this work, the proposed mixed-VT 3T GC-eDRAM is a viable alternative to SRAM for low power applications when compared to SRAMs in K. Sharma et al.and A. Goyal et al., taking up to 60-75% less space area and consuming 80-90% less power. By evaluating the cell in a memory array, it ran at a maximum frequency of 400 MHz and a DRT of 2.8µS at 85℃. It's refresh mode can be disguised in many applications because its availability exceeds 99% at 25℃. However, extensive research is required to determine the most efficient topology and sizing based on the application.

Acknowledgement

Authors would like to acknowledge the financial support of the Ministry of Higher Education (MOHE), Malaysia under the Fundamental Research Grant Scheme (FRGS) with Reference Code FRGS/1/2019/STG07/UTM/02/3 and Research University Grant (GUP) Project No. Q.J130000.3551.07G45. Also, thanks to the Research Management Center (RMC) of Universiti Teknologi Malaysia (UTM) for providing an excellent research environment in which to complete this work.

References

[1] K. C. Chun, P. Jain, and C. H. Kim, "Logic-compatible embedded DRAM design for memory intensive low power systems," ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems, vol. 1, pp. 277–280, 2010, doi: 10.1109/ISCAS.2010.5537877.

[2] P. Meinerzhagen, A. Teman, A. Mordakhay, A. Burg, and A. Fish, "A Sub- V T 2T Gain-Cell Memory for Biomedical Applications," vol. 1, no. d, pp. 1–3.

[3] Y. Zhang et al., "A batteryless 19 µw MICS/ISM-band energy harvesting body sensor node SoC for ExG applications," IEEE Journal of Solid-State Circuits, vol. 48, no. 1, pp. 199–213, 2013, doi: 10.1109/JSSC.2012.2221217.

[4] L. W. Stt-ram, M. Chang, P. Rosenfeld, S. Lu, and B. Jacob, "Technology Comparison for Large Last-Level Caches (L3Cs): Low-Leakage".

[5] W. K. Luk and R. H. Dennard, "2T1D memory cell with voltage gain," IEEE Symposium on VLSI Circuits, Digest of Technical Papers, no. CIRCUITS SYMP., pp. 184–187, 2004, doi: 10.1109/vlsic.2004.1346552.

[6] "International technology roadmap for semiconductors (2011). http://www.itrs.net/Links/2011ITRS/Home2011.htm."

[7] A. Burg et al., "A 4-stream 802.11n baseband transceiver in 0.13 µm CMOS," IEEE Symposium on VLSI Circuits, Digest of Technical Papers, pp. 282–283, 2009.

[8] M. T. Chang, P. T. Huang, and W. Hwang, "A 65nm low power 2T1D embedded dram with leakage current reduction," Proceedings - 20th Anniversary IEEE International SOC Conference, pp. 207–210, 2007, doi: 10.1109/SOCC.2007.4545459.
[9] J. Constantin et al., "TamaRISC-CS: An ultra-low-power application-specific processor for compressed sensing," IEEE/IFIP International Conference on VLSI and System-on-Chip, VLSI-SoC, vol. 07-10-Octo, pp. 159–164, 2015, doi: 10.1109/VLSI-SoC.2012.7332094.
[10] K. S. Michael Keating, David Flynn, Robert Altken, Alan Gibbons, Low Power Methodology Manual for System-on-Chip Design.
[11] A. Y. Dogan, J. Constantin, M. Ruggiero, A. Burg, and D. Atienza, "Multi-core architecture design for ultra-low-power wearable health monitoring systems," Proceedings -Design, Automation and Test in Europe, DATE, pp. 988–993, 2012, doi: 10.1109/date.2012.6176640.
[12] H. Abdo, N. E. Alias, A. Hamzah, I. Kamisian, M. L. Peng Tan, and U. U. Sheikh, "A 2 Kbit Memory Array of Mixed-VTGC-eDRAM Implemented in 130nm Standard CMOS Technology," Proceedings - 2021 IEEE Regional Symposium on Micro and Nanoelectronics, RSM 2021, pp. 153–156, Aug. 2021, doi: 10.1109/RSM52397.2021.9511591.
[13] A. Teman, O. Yadid-pecht, and A. Fish, "Leakage Reduction in Advanced Image Sensors using an Improved AB 2 C Scheme," no. September 2016, 2012, doi: 10.1109/JSEN.2011.2157123.
[14] N. Edri et al., "Silicon-Proven, Per-Cell Retention Time Distribution Model for Gain-Cell Based eDRAMs," vol. 63, no. 2, pp. 222–232, 2016.
[15] P. Meinerzhagen, A. Teman, R. Giterman, and A. Burg, "Exploration of Sub- V T and Near- V T 2T Gain-Cell Memories for Ultra-Low Power Applications under Technology Scaling," pp. 54–72, 2013, doi: 10.3390/jlpea3020054.
[16] R. Giterman, A. Teman, P. Meinerzhagen, A. Burg, and A. Fish, "4T Gain-Cell with Internal-Feedback for Ultra-Low Retention Power at Scaled CMOS Nodes," pp. 2177–2180, 2014.
[17] R. Giterman, A. Teman, A. Fish, and R. Gan, "A 11. 5pW / bit 400mV 5T Gain-Cell eDRAM for ULP Applications in 28nm FD-SOI," pp. 5–7, 2017.
[18] R. Giterman, A. Fish, N. Geuli, E. Mentovich, A. Burg, and A. Teman, "An 800-MHz Mixed- V T 4T IFGC Embedded Approximate Storage Applications," pp. 1–13, 2018.
[19] K. C. Chun, P. Jain, T. H. Kim, and C. H. Kim, "A 1.1V, 667MHz random cycle, asymmetric 2T gain cell embedded DRAM with a 99.9 percentile retention time of 110μsec," IEEE Symposium on VLSI Circuits, Digest of Technical Papers, pp. 191–192, 2010, doi: 10.1109/VLSIC.2010.5560303.
[20] E. V. Bravo, A. Bonetti, and A. Burg, "Data-Retention-Time Characterization of Gain-Cell eDRAMs across the Design and Variations Space," pp. 0–4, 2019.
[21] S. Ganapathy, A. Teman, R. Giterman, A. Burg, and G. Karakonstantis, "Approximate Computing with Unreliable Dynamic Memories," pp. 1–4, 2015.
[22] O. Maltabashi, H. Marinberg, R. Giterman, and A. Teman, "A 5-Transistor Ternary Gain-Cell eDRAM with Parallel Sensing," 2018.
[23] P. Meinerzhagen, A. Teman, A. Fish, A. Burg, and S. T. I. I. E. L. Tcl, "Impact of body biasing on the retention time of gain-cell memories," pp. 1–4, 2013, doi: 10.1049/joe.2013.0057.
[24] C. S. Savalam, K. Prasanti, and A. S. Haranath, "Design and implementation of high performance and low power mixed logic line decoders," International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 6, pp. 635–640, 2019, doi: 10.35940/ijitee. F1131.0486S419.
[25] A. Kumar Mishra, "Design of Novel Address Decoders and Sense Amplifier for SRAM Based Memory," no. May 2014.
[26] K. Sharma, M. Mehta, and S. Tyagi, "Design and Performance Analysis of 6T SRAM on 130 nm Technology," 2019 International Conference on Signal Processing and Communication, ICSC 2019, pp. 363–368, 2019, doi: 10.1109/ICSC45622.2019.8938162.
[27] P. Meinerzhagen, A. Teman, R. Giterman, A. Burg, and A. Fish, "Exploration of sub-VT and near-VT 2T gain-cell memories for ultra-low power applications under technology scaling," Journal of Low Power Electronics and Applications, vol. 3, no. 2, pp. 54–72, 2013, doi: 10.3390/jlpea3020054.
[28] A. Goyal and V. K. Agarwal, "Low Power Consumption Based 4T SRAM Cell for CMOS 130nm Technology," Proceedings - 2016 8th International Conference on Computational Intelligence and Communication Networks, CICN 2016, pp. 590–593, 2017, doi: 10.1109/CICN.2016.121.
[29] K. C. Chun, P. Jain, T. Kim, C. H. Kim, and S. Member, "A 667 MHz Logic-Compatible Embedded DRAM Featuring an Asymmetric 2T Gain Cell for High Speed On-Die Caches," vol. 47, no. 2, pp. 547–559, 2012.
[30] D. Somasekhar et al., "2 GHz 2 Mb 2T Gain Cell Memory Macro With 128 GBytes / sec Bandwidth in a 65 nm Logic Process Technology," vol. 44, no. 1, pp. 174–185, 2009.
[31] Y. S. Park, D. Blaauw, D. Sylvester, and Z. Zhang, "Low-power high-throughput LDPC decoder using non-refresh embedded DRAM," IEEE Journal of Solid-State Circuits, vol. 49, no. 3, pp. 783–794, 2014, doi: 10.1109/JSSC.2014.2300417.