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Device Characterization of 0.21 µm CMOS Device

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Abstract

The objective of this study was ot measure the electrical characteristics, observe the structure and characterize the material of 0.21µm CMOS devices. The material characterization of the 0.21µm CMOS devices were carried out using FIB milling technique, SEM surface morphology and EDX Analysis. The CVIV tester was used for electrical characterization of the device. All the IDVD and IDVG graphs obtained are similar to the standard graph. There are two ways to calculate the devices VTH manual calculation method and auto calcualtion method. Calculation of the VTH by using the manual calcuation method was found to be more accurate than the auto calcuation method. The VTH value for NMOS and PMOS obtained from this study is 0.398393 AND -0.715700. Both these values are compared with the standard VTH value from Silterra, where this calculation involved polynomial regression technique in MATLAB. It is found that, the tested PMOS devices are practical but the tested NMOS devices are not. The materials used to fabricate this device has been obtained and shown. The electrical and material characteristics of the 0.21µm CMOS devices are successfully characterized by using the above methods.

Keywords: CMOS, EDX, FIB, SEM, electrical and material characterization, polynomial regression technique

1 INTRODUCTION

A. Types of MOSFET

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a transistor consists of metal (gate), oxide (insulator between semiconductor substrate and metal gate), and semiconductor (substrate, source, and drain). Figure 1 shows a typical MOSFET structure. As the technology growth, the metal is replaced by polysilicon as polysilicon has the ability to reduce the threshold voltage value and sustain high temperature in post-implantation annealing process (Hong Xiao 2001, I.Ahmad et al. 2002). There are two types of MOSFETs (a) n-type MOSFET (NMOS), and (b) p-type MOSFET (PMOS). If the current from the source to drain is carried by electron, it is defined as NMOS, while if the current from the source to drain is carried by holes it is defined as PMOS. Fig 2 and Figure 3 show the structure and symbol of a NMOS and PMOS respectively.

Complementary MOS (CMOS) refers to complementary p-type MOSFET and n-type MOSFET pair as shown in Figure 4. CMOS logic is the most popular technology utilized in present-day integrated circuit design. The main reasons for the success of CMOS are low power consumption and good noise immunity (Oldham 2002, B.Y.Majlis 2000). Currently CMOS technology is used in advanced integrated circuit manufacturing due to the low power dissipation requirement.

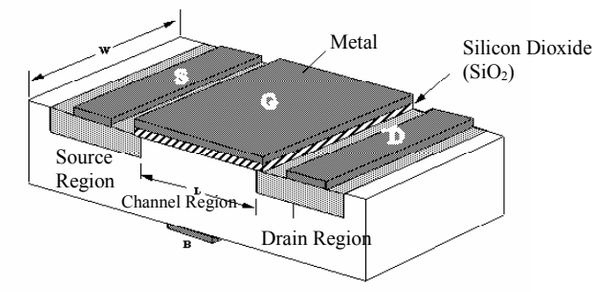


Figure 1. A typical MOSFET structure.

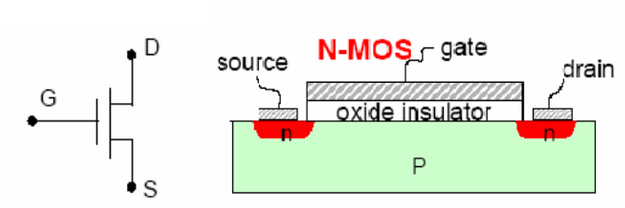


Figure 2. The circuit symbol and structure of NMOS.

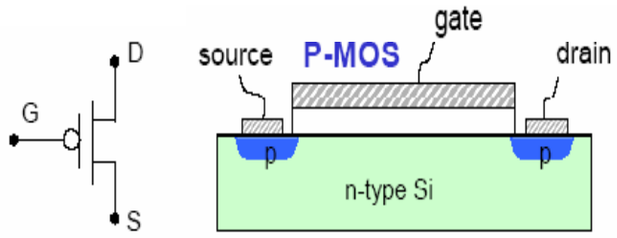


Figure 3. The circuit symbol and structure of PMOS.

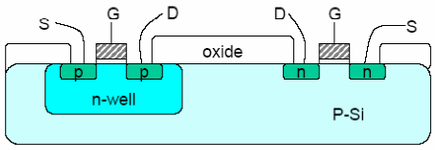


Figure 4. CMOS structure that consists of NMOS and PMOS on the same substrate.

B. Focused Ion Beam (FIB) Milling Technique

The operation of a FIB begins with a liquid metal ion source (LMIS). A reservoir of Gallium, Ga is positioned in contact with a sharp Tungsten (W) needle. The Ga wets the needle and flows to the W tip. A high extraction field (>108 V/cm) is used to pull the liquid Ga into a sharp cone whose radius range from 5–10 nm. Ions are emitted as a result of field ionization and post-ionization and then accelerated down to the FIB column. The use of Ga is advantageous for two reasons: (i) Ga has a low melting point and, therefore, exists in the liquid state near room temperature, and (ii) Ga can be focused to a very fine probe size (<10 nm in diameter). FIBs typically operate with an accelerating voltage between 5 to 50 keV. By controlling the strength of the electrostatic lenses and adjusting the effective aperture sizes, the probe current density (and therefore, beam diameter) can be altered from tens of pA to several nA corresponding to a beam diameter of 5 nm to 0.5 ¼m (Giannuzzi 1999).

The sputtering process is important for a knowledgeable operation of the FIB. When a Ga+ ion is accelerated toward the target sample, it enters the sample and creates a cascade of events, which results in the ejection of a sputtered particle (which may be an ion or a neutral atom). This sputtering mechanism thus 'cut' the device and provide sample for the SEM analysis.

C. Scanning Electron Microscope (SEM)

The major concepts, which lead to the development of electron microscopy, is "any particle can exhibit wave character" (The de Broglie hypothesis). Later it became fact that, magnetic or electrostatic fields can be used to focus electrons.

The operating principle in this instrument was focusing an electron beam as a spot on the sample to be investigated, and scanning this spot across the sample surface. Each point struck by the spot was produced a response that was collected and displayed to give an image (As shown schematically in Figure 5).

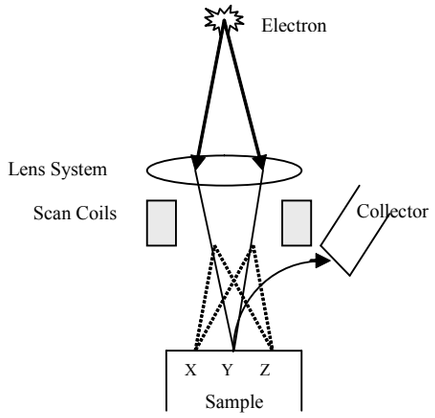


Figure 5. Schematic operating principle of a scanning electron microscope.

D. Field Emission Scanning Electron Microscope (FESEM)

FESEM is the abbreviation of the word Field Emission Scanning Electron Microscope. Scanning and electron transmission microscopes (SEM and TEM) are used as a source for image formation electrons (particles with a negative charge), in contrast to light microscopes (LM). These electrons are produced by a field emission source in a FESEM. The sample (object) is scanned in a kind of zigzag pattern by an electron beam. Its principle is almost like the SEM but it can have a better resolution images.

E. Energy Dispersive X-rays (EDX) Analysis

Normally, a SEM unit is used for monitoring the cross-section area of the CMOS device (sample), whereas the composition of the sample can determine qualitatively by EDX analysis build in unit.

During EDX analysis, the specimen is bombarded with an electron beam inside the scanning electron microscope. The bombarding electrons collide with the specimen atom's electrons, knocking some of them off in the process. A higher-energy electron from an outer shell eventually occupies a position vacated by an ejected inner shell electron. To make this possible, however, the transferring outer electron must give up some of its energy by emitting an X-ray. The amount of energy released by the transferring electron

depends on which shell it is transferring from, as well as which shell it is transferring to. Furthermore, the atom of every element releases X-rays with unique amounts of energy during the transferring process. Thus, by measuring the amounts of energy present in the X-rays being released by a specimen during electron beam bombardment, the identity of the atom from which the X-ray was emitted can be established.

The output of an EDX analysis is an EDX spectrum. The EDX spectrum is just a plot of how frequently an X-ray is received for each energy level. An EDX spectrum normally displays peaks corresponding to the energy levels for which the most X-rays had been received. Each of these peaks is unique to an atom, and therefore, corresponds to a single element. The higher a peak in a spectrum, the more concentrated the element is in the specimen. Therefore, the precise element composition of the material can be obtained.

2 EXPERIMENT PROCEDURE

The purpose of the study was to measure the electrical characteristics, observe the structure and characterize the material of 0.21µm CMOS devices. The electrical property characterization and material characterization were conducted using the following procedure.

A. Electrical Property Characterization

The CVIV measurement system consists of four probes manipulators, which consist of BNC cable and probe needle, a microscope, and wafer plate, measurement equipment (tester – in this case using Keithley 236 Source Measuring Unit, SMU) that are connected to software (PC Controller) using IEEE cable, light and vacuum tube.

The device was placed on the wafer plate which had vacuum tube to suck the wafer down to its place. The plate was placed right under the microscope to view the cross section of the device. Then the probes touch the four terminal of the device namely the source, drain, gate and substrate. After putting some voltages to the gate and drain while the source and substrate grounded, the current-voltage (I-V) graph was obtained using ICS software.
Test conditions were as follows;
For IDVG:
VG = 0 to 3.3 V (Sweep from 0 V until 3.3V)
VD = 0.1V (Constant)
VS = Vsubstrate = Gnd

With the mentioned test conditions, ID is measured and IDVG curve is plotted. Then VTH is calculated from the curve.

For IDVD:
VG = 1 – 3 V (Step voltage for 1V, 2V and 3V)
VD = 0 to 3.3 V (Sweep from 0 to 3.3V)
VS = Vsubstrate = Gnd
The ID is measured and IDVD curve is plotted. Then the obtained curve's shape was compared with the standard IDVD curve.

B. Material Characterization

In this section, the sample must be prepared before being tested. The equipment that was used was microscope, diamond cutter, FIB, FESEM, and SEM with EDXA built-in unit. The diamond cutter was used to cleave the wafer to become smaller pieces. The steps for wafer cleaving by using the diamond cutter to prepare the sample for FIB are shown in Figure 6.

After the wafer had been cleaved, the sample was cross-sectioned to prepare for the EDX analysis. The cross-section of the sample was prepared by using the FIB. The sample needed to be cross-sectioned was put in a chamber and the chamber pressure was reduced to 1.8 x 10-7 milibar. There are two modes of milling process for cross-sectioning, which is rough milling (2700pA) and fine milling (300-1000pA). Initially, the rough milling was used because it can mill faster and it was followed by the fine milling. Here, the depth that could be milled was around 3µm from the sample's surface. After the cross-section has been made, the CMOS structure was obtained not very clear nonetheless. Thus, the devices cross-section had are taken from the FESEM where the pictures obtained from the FESEM were clearer and sharper.

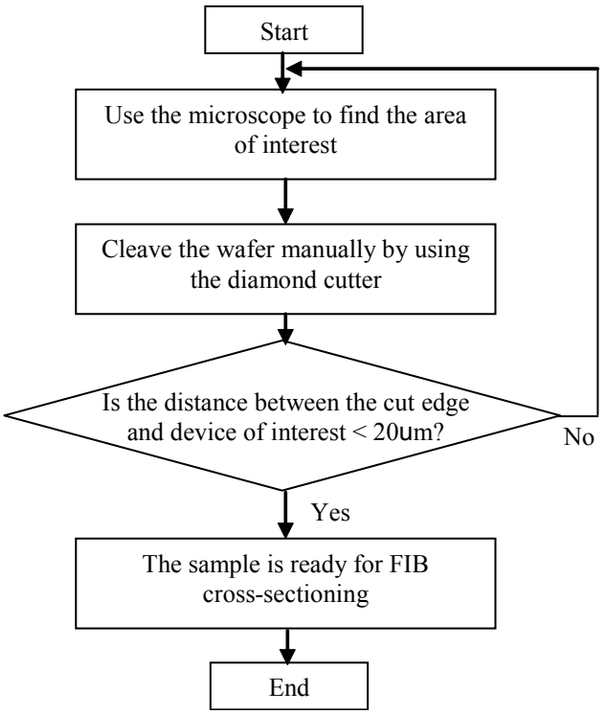
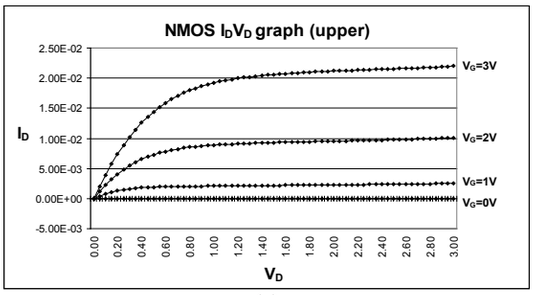


Figure 6. The flow chart of steps wafers cleaving.

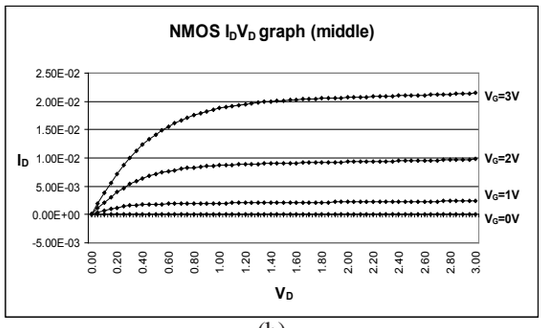
Characterization of the elements and composition in the devices were carried out by the EDX analysis (EDXA). EDXA was done by measuring the energy or wave length and the intensity distribution for the X-rays signal that was generated from the electron beam that focused at the specimen. With the EDXA, the actual elements composition for the materials in different areas can be obtained from the X- Rays spectrum.

3 RESULTS

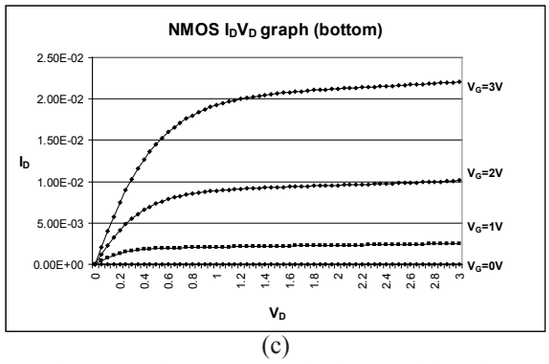
A. Results for Electrical TestFigure 7(a), 7(b) and 7(c) show the IDVD graphs for NMOS at the upper, middle and bottom part of the wafer, respectively. Each IDVD graph contains four different curves. The applied VG are different and their values are between 0 to 3V.



(a)



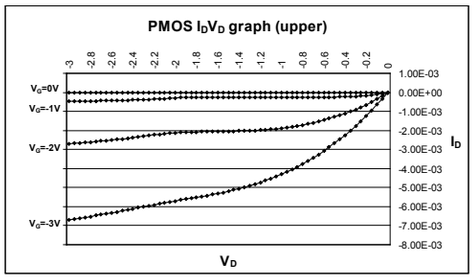
(b)



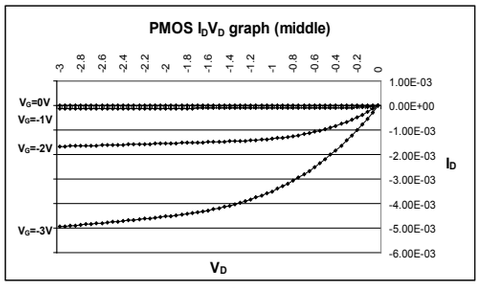
(c)

Figure 7. The IDVD graphs for NMOS at the
(a) upper,
(b) middle and
(c) bottom part from the wafer.

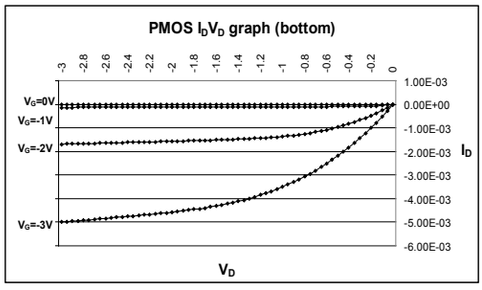
Figure 8(a), 8(b) and 8(c) show the IDVD graph for PMOS at the upper, middle and bottom part of the wafer, respectively. Each IDVD graph contains four different curves. The applied VG are different and their values are in between -3 to 0V.



(a)



(b)



(c)

Figure 8. The IDVD graphs for PMOS at the
(a) upper,
(b) middle and
(c) bottom part of the wafer.

Figure 9 shows the NMOS IDVG graph at the upper part of the wafer. The VTH manual and auto calculation are shown in Figure 10. By using the same method VTH values are calculated for all the NMOS and PMOS from upper, middle and bottom part of the wafer. All the VTH values are shown in Table 1.

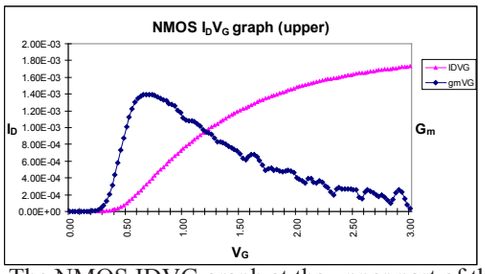


Figure 9. The NMOS IDVG graph at the upper part of the wafer.

V_{TH} Manual	V_{TH} Auto
$V_{TH} = V_{G\max} - \frac{I_{d\max}}{\text{gm}} - \frac{V_d}{2}$	$V_{TH} = X\text{int} - \frac{V_d}{2}$
$V_{TH} = 0.7 - \frac{0.00035755}{0.0013972} - \frac{0.1}{2}$	$V_{TH} = 0.43826 - \frac{0.1}{2}$
$V_{TH} = \underline{\underline{0.39409}}$	$V_{TH} = \underline{\underline{0.38826}}$

Figure 10. The VTH manual and auto calculation.

Table 1 The manual and auto values of VTH for NMOS and PMOS from upper, middle and bottom part of the wafer.

Part/ location	NMOS		PMOS	
	V_{TH} Manual	V_{TH} Auto	V_{TH} Manual	V_{TH} Auto
Upper	0.39409	0.38826	-0.69416	-0.69430
Middle	0.40240	0.39794	-0.72995	-0.72991
Bottom	0.39869	0.39869	-0.72299	-0.72291

In order to choose which calculation method should be used; the sample variance (S2) for the VTH manual and auto are calculated by using this formula:

Where, n is the number of sample; is the sample mean.

Table 2 shows the sample variance and standard deviation (S) of VTH manual and auto for NMOS and PMOS. Here, the standard deviation (S) is the square root of sample variance.

Table 2 The sample variance (S2) and standard deviation (S) of VTH manual and auto for NMOS and PMOS.

Calculation method	NMOS		PMOS	
	Sample variance (S^2)	Sample standard deviation (S)	Sample variance (S^2)	Sample standard deviation (S)
V_{TH} Manual	0.0000173	0.004163	0.00036	0.018976
V_{TH} Auto	0.00003384	0.005817	0.000356	0.018866

B. Results for material test

A cross-section structure of the CMOS device is shown in Figure 11. According to this figure, analysis EDX can be performed at different locations in the CMOS device structure. Finally, after each area (number 1-7) is analyzed, the materials that consist in the devices can be obtained. In EDX analysis, each location at the structure was tested three times to obtain a more accurate data to represent or support for the same material.

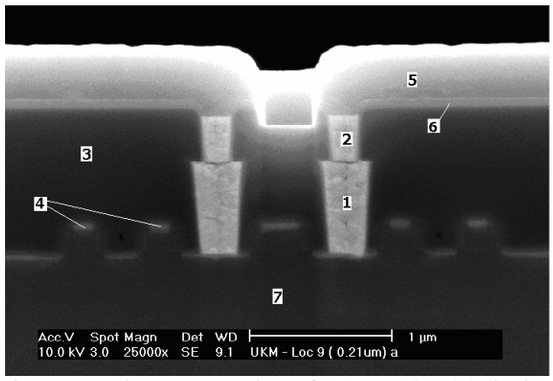
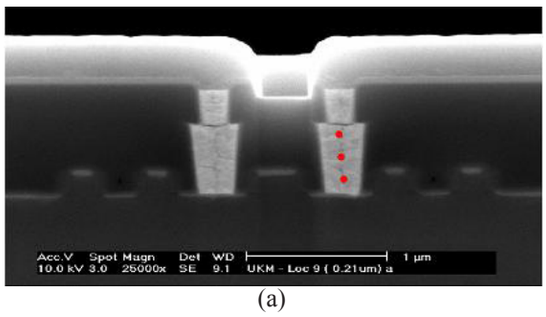


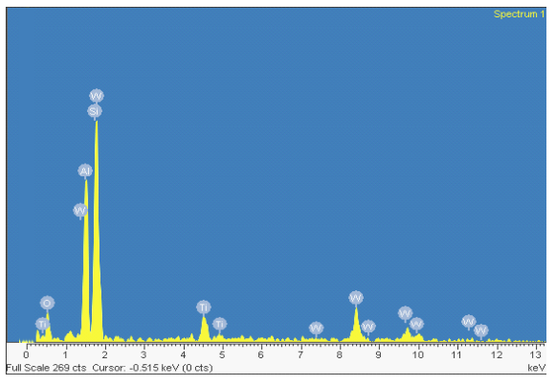
Figure 11. The cross-section of 0.21µm CMOS device.
Number 1-7 represent the different locations that have been tested.

Figure 12 shows the EDX data obtained from the area denoted as 1 in Figure 11. In Fig 12, the sampling points are shown in (a); the related EDX spectrum is shown in (b). The average values of weight in percentage are shown in Table 3 and Figure 13.

After analyzing the obtained data, the material at the area No. 1 is determined as Tungsten (W).



(a)



(b)

Figure 12. (a) Sampling area (the spots represent sampling point);
(b) One of the spectrum from the sampling point in (a).

Table 3 Results from area that denoted as 1 in Figure 11.

Element	Reading			Total %	Average %
	1	2	3		
O	12.24	19.65	21.79	53.68	**17.89**
Al	20.71	22.35	17.77	60.83	**20.28**
Si	13.06	23.66	25.02	61.74	**20.58**
Ti	15.33	10.73	8.18	34.24	**11.41**
W	29.65	23.61	27.24	80.50	**26.83**

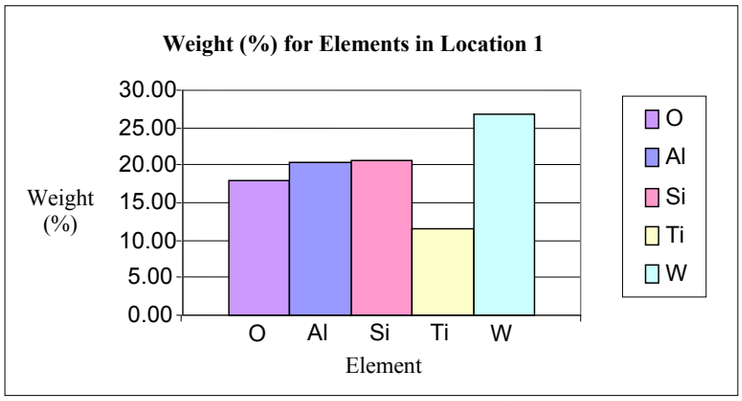


Figure 13. Bar chart show the percentage weight of the area denoted as 1.

Each area (number 1-7) of the CMOS structure was analyzed and their average percentage weight was calculated. Table 4 summarized the material that consists in the CMOS devices.

Table 4 The material consists in the CMOS structure from No.1-7 in Figure 11.

Area denoted	Material
1	Tungsten (W)
2	Aluminium (Al)
3	Dielectrics (SiO_2)
4	Polysilicon (Si)
5	Aluminium (Al)
6	Aluminium (Al)
7	Silicon (Si)

4 DISCUSSION

A. Results of electrical characteristics

All IDVD graphs for NMOS and PMOS were compared to the standard graph. The graphs obtained were similar to the standard graph (Sze 2002). This show that the tested devices were functioning well and the method used in this study was suitable.

Table 2 indicated that the manual VTH calculation method have smaller data variability than the auto VTH calculation method. This could be due to the S2 value for the manual VTH calculation method being smaller than

the auto generated. If the S2 is small, the variability in data will also be small. Consequently, if S2 is large, the variability in data is large (Dauglas et al. 2004). Therefore, the VTH value should be calculated by using the manual calculation method. The VTH value obtained for the NMOS and PMOS is 0.398393 and -0.715700 respectively.

In order to determine that the VTH value is practical, the obtained VTH values are compared with the standard VTH value from Silterra Malaysia, the supplier of the sample. Table 5 shows the standard VTH value from Silterra (Silterra 2006). From the table, it can be seen that the tolerance was approximately 12.7% for both the NMOS and PMOS. Since the VTH value for 0.21µm CMOS devices is not given, the polynomial regression technique in MATLAB is used to calculate the standard VTH value so that it can be compared with the results obtained from the study.

The standard VTH value for 0.21µm device calculated from the polynomial regression technique is shown in Table 6, Table 5 was used as the input for this calculation technique. As can be seen from Table 6, the VTH value for NMOS and PMOS were not in the range of 0.5253± 12.7% for NMOS and -0.6907± 12.7% for PMOS; the devices would be not practical. The VTH value from this experiment was then compared to the standard VTH value. The standard VTH value range for NMOS and PMOS were calculated and the ranges are as shown in Figure 14.

Table 5 Standard VTH value for 0.13, 0.18 and 0.22µm CMOS devices from Silterra.

Transistor size (nm)	NMOS V_{TH} value (V)	PMOS V_{TH} value (V)
130	0.34± 12.7%	-0.34± 12.7%
180	0.42 ± 12.7%	-0.50 ± 12.7%
220	0.57 ± 12.7%	-0.77 ± 12.7%

Table 6 Standard VTH value for 0.13, 0.18, 0.21 and 0.22µm CMOS devices from Silterra. (Note that the data for 0.21µm is obtained from polynomial regression technique in MATLAB).

Transistor size (nm)	NMOS V_{TH} value (V)	PMOS V_{TH} value (V)
130	0.34± 12.7%	-0.34± 12.7%
180	0.42 ± 12.7%	-0.50 ± 12.7%
210	**0.5253± 12.7%**	**-0.6907± 12.7%**
220	0.57 ± 12.7%	-0.77 ± 12.7%

The calculation of standard VTH value range for NMOS and PMOS are as follows:-

VTH value for 0.21µm NMOS:

VTH = 0.5253V ± 12.7%

= 0.4586V d" VTH d" 0.5920V

VTH value for 0.21µm PMOS:

VTH = -0.6907V ± 12.7%

= -0.6030V d" VTH d" -0.7784V

In the experiment, the VTH value for NMOS and PMOS are as follows:-

For 0.21µm NMOS:

VTH = 0.398393

For 0.21µm PMOS:

VTH = -0.715700

By comparing the results between standard VTH value and the experiment from the calculation above, it was found out that the VTH value for PMOS was in the range but the NMOS was out of the range. This shows that the PMOS is practical but the NMOS is not because its VTH value is less than the minimum standard value from Silterra.

B. Results of material characteristics

Figure 11 is used for explanation in this section. Generally, area No. 1 is a contact hole or via. Tungsten (W) is the material that is commonly used to fill this hole and form the plug to contact the metal and silicon layer or between different metal layer (Hong Xiao 2001). Area No. 2 is Aluminum (Al) that is used as metal interconnections. Silicon dioxide (SiO2) is used as dielectric layer for area No. 3.

Generally, gate transistor is made from polysilicon (I.Ahmad 2002) because it can sustain high temperature during the post-implantation annealing process (Hong Xiao 2001). Thus, polysilicon (Si) is the material used in the area No. 4. Area No. 5 and 6 are the metal layers that formed by Aluminum (Al), but with different weight percentage. From the obtained data, the weight percentage for Al in area No. 6 was higher than in area No. 5. The value was 61.63% for area 6 and 51.67% for area 5.

Area 7 in the transistor cross-section is the substrate for the transistor; normally it is made up by bulk silicon. Results show that this area is form by silicon and its weight percentage is 100%.

5 CONCLUSION

The electrical and material characterization of the 0.21µm CMOS devices has been successfully characterized by using the FIB, FESEM, EDX analysis and CVIV Measurement System. The entire IDVD graphs obtained from the experiment is similar to the standard IDVD graph. It was found that the manual VTH calculation method was more accurate than the auto method because its sample variance (S2) was smaller. Thus, the VTH value for NMOS and PMOS is 0.398393 and -0.715700, respectively. Both VTH values were compared to the standard VTH value from Silterra. It was discovered that the PMOS was practical but the NMOS was neither practical nor applicable. Hence, from the spectrum analysis by EDX, the material composition indicates the exact chemical and physical properties.

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