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The Effect of Nanowire Gap for Silicon Nanowire Transistor to the Current-Voltage (I-Vds)

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Keywords

Silicon nanowire transistor, local anodic oxidation, nanowire gap

Abstract

One-dimensional structures are attracting a lot of attention for optimizing applications as one of the most sensitive devices. Among the fabricated devices, silicon nanowires (SiNW) and silicon nanowire transistors (SiNWT) are of particular importance for promising applications fabricated using bottom-up or top-down approaches to nanoscale devices. In this paper, the sensitivity of the current-voltage characteristic to the nanowire gap of a silicon nanowire transistor (SiNWT) was analyzed. SiNWTs with different nanowire gaps were fabricated using scanning probe microscopy by local anodic oxidation (LOA). Varies gaps can be occurring during the fabrication processes and its can be controlled by RASTER programming in LAO. These gaps can give different results of the sensitivity to the volt-ampere response. However, these gaps can be neglected depending on the subject of the studies and important to the other study, especially in nano particle sensors. In this experiment, the nanowires gaps were developed in the range of 100.5-435.6 nm and had been plotted the measurement data with the volt-ampere response. The data was analyzed using a semiconductor analyzer connected to a HP 4156C SPA series software analysis model from Desert Cryogenics. From the results had been measured the Current-Voltage (IV) increases proportionally with the nanowire gap distance in the SINWT device and this results will give significant effects to the application in nanoparticle sensors.

1. Introduction

Silicon nanowire transistors (SiNWs) have become essential parts in the evolving field of nanoelectronics, providing unmatched prospects for miniaturization and performance improvement. SiNWs are excellent prospects for future-oriented electronic devices because they display distinctive electrical properties and are distinguished by their nanoscale size. The nanowire gap, which is an inherent characteristic that symbolizes the distance between the source and drain electrodes, stands out as a crucial factor that requires careful study

among the countless factors dictating the behavior of SiNW transistors. Researchers now have the ability to accurately control and change the nanowire gap with remarkable accuracy, thanks to recent developments in nanofabrication techniques, which has necessitated a thorough investigation of its impact on SiNW transistor performance. By exploring the convoluted connection between the nanowire gap and the current-voltage (I-V) properties of SiNW transistors, this study seeks to close this knowledge gap. SiNW transistors must be optimized for use in a variety of applications, and this requires an extensive knowledge of how changes in the nanowire gap dimension affect the device's I-V properties. Researchers hope to open up novel design options, improve device performance, and enable customized solutions for many electronic platforms, from energy efficient IoT sensors to high-performance computer systems, by explaining this fundamental relationship.

The study's results on the intricate relationship between the I-V properties of SiNW transistors and the nanowire gap are presented in this publication, adding to the expanding reservoir of knowledge in the field of nanoscale electronics and offering practical suggestions for the design and improvement of future gadgets. The article demonstrates how the nanowire gap influences the characteristics of SiNW transistors by utilizing the most recent findings and methodologies, which are built upon a foundation of cutting-edge research. The relevance of nanowire gap optimization for ultra-sensitive detection was recently highlighted by Zhang et al., who demonstrated the amazing sensitivity of SiNW transistors in bio sensing applications [1]. Furthermore, the work done by Chen and Li in 2023 on SiNW field-effect transistors in integrated circuits emphasizes how crucial perfect gap control is to achieve high-speed data processing [2]. The study by Wang and Xu also investigates cutting-edge fabrication techniques for SiNW transistors, offering revolutionary techniques for nanowire gap engineering [3]. Additionally, the flexibility of SiNW transistors for future electronics was highlighted by Kim and Park's research, which looked at how to incorporate them into flexible electronic platforms [4].

The advancement of new technologies is explained by the remarkable scale of miniaturization to ultra-micro sizes [5]. It is the fundamental principle of nanotechnology that has penetrated the fields of applied sciences, manufacturing, industry, military, medicine, agriculture and other fields [6]. The most notable examples are in the fields of nanoelectronics and nanoscience, where technological advances have been made by shrinking and miniaturizing transistors and adding transistors for microchips [7]. With the recent advent of the Internet of Things (IoT) [8], sensors have become an essential component for monitoring and continuously monitoring various physical stimulus parameters and updating information to the Internet [9,10]. Due to their distinct mechanical, electrical, and optical characteristics, silicon nanowires have emerged as one of the most promising measuring and monitoring techniques [11]. Due to its ultra-sensitive, selective, real-time, and label-free detection capabilities, silicon nanowire field-effect transistors (Si-FET) have attracted a lot of interest as prospective instruments for studying molecules that interact with or are connected to sensors [12]. SiN-FETs are the perfect nanosensor due to their special characteristics, which include tiny size, light weight, low cost, flexibility, quick response, stability, and scalability [13]. The Silicon Nanowire Transistor (SiNWT), which is likely to be the successor to FET-based nanoscale devices, is a basic device that is used in the performance research of simplicity and complexity. However, the parameters of the SiNWT (channel length, diameter, nanowire size, and nanowire gap) are impacted and the performance of the transistor degrades when the SiNWT's dimensions (length and diameter) decrease [14]. These SiNWTs can be optimized as prospective research instruments for bio molecular interactions and electro covalent interactions because of their ultrasensitive, selective, label-free detection capabilities, as highlighted in several literature publications [12]. Due to SiNW's direct charge buildup in the material's bulk, which causes a quick detection response, it demonstrated strong electron transmission during detection at the lowest dimensions [11]. According to the SiNW dimensions, which range from 1-100 nm, these scales are extremely equivalent to and consistent with those of biological and chemical species [15,16].

Integrating this research study with the most recent advancements in the field of nanoscale electronics, this article emphasizes new results on the intricate connection between the nanowire gap and the I-V properties of SiNW transistors. Future SiNW transistor designs will benefit from this study's significant expertise, which will help with application growth and performance improvement.

2. Material and Methods

The instruments used in this study are Atomic Force Microscopy (AFM) chamber for transistor patterning using AFM nanolithography (SII Nanotechnology, SPA300HV). The electrical characterization using a semiconductor parameter analyzer (SPA) linked to the Desert Cryogenics HP4156 CSPA series software analysis model. Image characterizations are using Scanning Electron Microscope (Fe-SEM) model XHR Extreme High Resolution Field Emission Scanning Electron Microscope (XHR-FESEM) Model FEI Verios 460L. Materials used in this study are p-type, silicon insulator (SOI) wafer (Shin-etsu, Japan) resistivity 510 Ωm, Si layer thickness ~ 70 nm, SiO_2 thickness ~ 2000 nm as a main substrate for the device. Potassium hydroxide (KOH) pellets, Isopropyl alcohol (2- Propanol) with purity 99.8%, Di-ionize water (DIW), flask 25 mL, 50 mL and 100 mL and a watch glass.

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3. Experimental Procedures

The fabrication of the masking device will be the initial step in the experimental method. A sample of a p-type silicon insulator (SOI) wafer with resistivity of 510 m, a Si layer thickness of 70 nm, and a SiO2 thickness of 2000 nm must be prepared first. The samples were cut into squares that were around 1.5 cm by 1.5 cm in size. Following the steps of the RCA1 and RCA2 techniques, the samples were next washed using conventional washing procedures (Radio Company of America). This removed both organic and non-organic pollutants. As explained by Kern, W in 1990, the RCA clean process is renowned for its efficiency in delivering a high level of cleanliness and surface preparation for following semiconductor production procedures, and it has since become the industry standard cleaning procedure for Silicon wafer [17]. The native oxides are subsequently eliminated using hydrofluoric acid (HF) that has been 1:80 diluted in deionized water (DIW). These procedures make sure that all of the beginning circumstances for the produced sample are the same throughout. The sample was cleaned before proceeding into an Atomic Force Microscopy (AFM) chamber to be used for AFM nanolithography (SII Nanotechnology, SPA300HV), which is used to shape transistors. On the silicon on insulator (SOI), all necessary parameters are set up in the AFM mode as needed for continuous procedures. The transistor circuit will be built as seen in Fig. 1. For vector scanning applications, design commands were used in raster programming, which is compatible with the abovementioned AFM design.

Nanowire gap variation is defined by giving commands by writing a command language or by placing coordinates in auxiliary sub consoles at X and Y positions. The commands from the programming and/ or coordinates placing in sub-console or vice versa are depends on user to achieve the gap on nanowire fabricated. The parameters of the vector scanning design by local anodization (LAO) via AFM nanolithography are parameters that must be considered when creating various gaps of the SiNWT. The commands in the X and Y position sub-window and raster programming in the vector scan window, as seen in Figs. 2 and 3, can both be used to adjust the gap variation. With a complete comprehension of the instruction, both alterations can provide the intended outcomes. Both commands in Fig. 2 and Fig. 3 are correlated to each other to set the desired gap for the final outcomes as shows in colored flow chart box in Fig.4. After that the process of device fabrication was continued for etching process, the fabricated sample is further etched using KOH solution in the ratio 30% by weight was added to the mixture at 10% volume IPA. The mixture of 10% volume IPA was measured to get the simplicity of the ratio, since the KOH solution already diluted in DIW in the first stage. Etching conditions were maintained at a temperature of 65° C±3°C, and the etching time was around 17-19 seconds while stirring the solution at a speed of 500 rpm. Since the thicknesses of the mask from the early process are too thin, the difference of 1-2 seconds is crucial. Once the tolerance is more than 2 seconds, the etching solution will over have etched the desired structure. Then, the samples were washed with DIW for at least 1 min. This process is to remove the oxide mask by etching this sample again with a 1:80 dilution of HF:DIW to obtain the final structure. Here, the etching time is ~20sec at room temperature. The sample is then subjected to preliminary morphological and electrical characterization, which the entire of these processes are shows in Fig. 4.

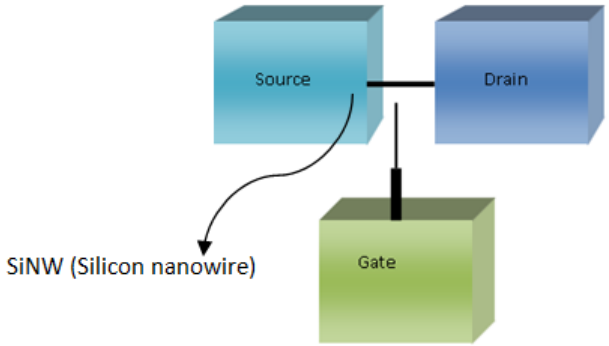

Fig. 1 *Illustration of silicon nanowire transistor (SiNWT)*

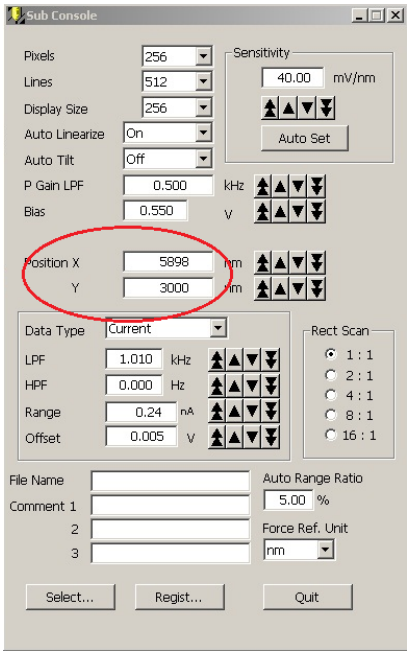

Fig. 2 *Auxiliary console window for setting coordinates along the X and Y axes*

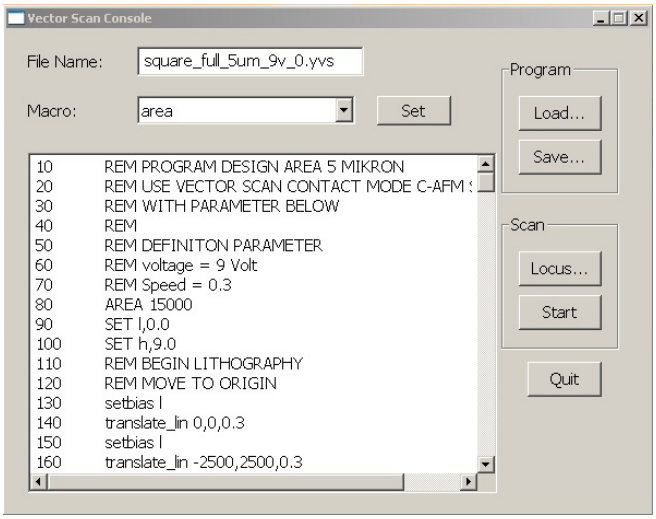

Fig. 3 *Loading raster programming in a vector scan console window*

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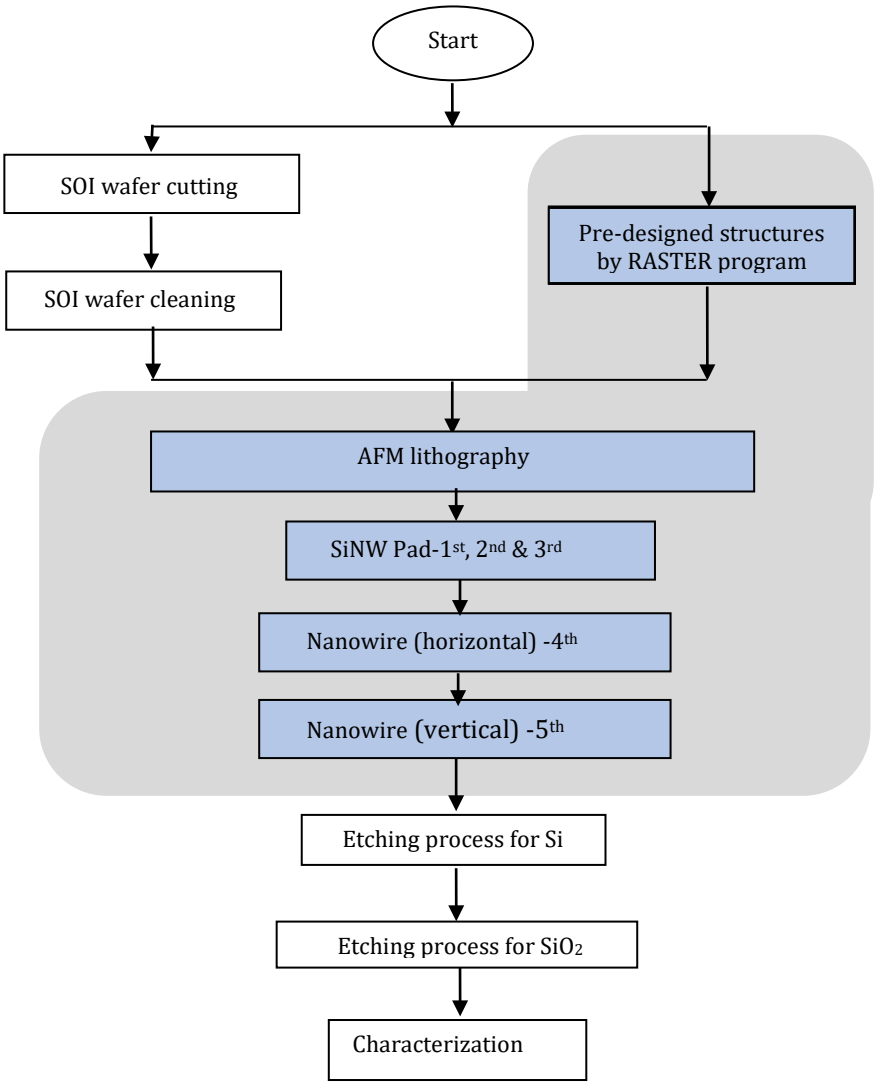


Fig. 4 *The entire process for fabrication of SiNWT*

4. Result and Discussions

In the pursuit of enhanced precision and minimized structural errors in Silicon Nanowire Transistor (SiNWT) devices, this experimental study adopted a meticulous approach focused on controlled partial fabrication. The primary objective was to effectively manage the nanowire gap within the completed SiNWT structure. To achieve this, the fabrication process was divided into discrete segments, and a mask structure was systematically developed using Local Anodic Oxidation (LAO) on the wafer. The wafer was subdivided into five distinct regions, corresponding to sequential steps in the SiNWT fabrication process (termed as the 1st step to the 5th step), as mentioned in method of fabrication in Fig. 4 while resulted in Fig. 5. Each structural element, including the device's pads and nanowires, underwent the LAO technique separately and in order. This step-by-step process required the controlling programme to receive exact command inputs, specifically within an auxiliary sub-window. The X and Y coordinates were methodically modified to precisely traverse the LAO procedure. This approach is consistent with current developments in nanofabrication methods. Additionally, it is influenced by comparable research that has used segmented fabrication to improve nanoscale device designs. For instance, Smith et al.'s study from 2023 showed the benefits of segmented fabrication for nanowire-based sensors, displaying improved device functionality. Zhao and Chen in 2022, also investigated the exact control of nanowire alignment in segmented fabrication processes, emphasizing its significance in nanoelectronics [18].

The Local Anodic Oxidation (LAO) process was methodically carried out in a segmented method, including resting intervals for the Atomic Force Microscope (AFM) between each step, in the goal of accurate and optimized SiNWT device construction. Even though it took a long time, this method was crucial for reaching the ideal structural quality and cleanliness. To ensure that every part of the SiNWT gadget achieved its optimum condition, cautious coordination was required due to the employment of special instructions contained in RASTER programming. On the other hand, the chance of obtaining clean and ideal structures was significantly reduced when longer instructions were used, covering every aspect of the fabrication process in a continuous

sequence. This phenomenon is caused by complex elements and complexities, which is this topic that has been thoroughly investigated in previous study [13]. Figs. 6(a), (b), (c), and (d) show SEM micrograph pictures of the finished SiNWT structures with various nanowire gap diameters, vividly illustrating the results of this strategy. According to recent developments in nanofabrication methods, these pictures provide visible confirmation of the crucial roles that segmented fabrication and AFM resting intervals played in obtaining the requisite structural integrity and cleanliness. The research of Lee et al. in 2023, which emphasized the relevance of regulated fabrication intervals in the optimizing of nanowire-based devices, serves as an example of how this study builds upon and validates earlier research results [19]. Additionally, Zhang and Wang in 2022 investigated the subtle elements impacting structural quality in segmented fabrication processes, offering insightful information on the efficiency of this technology [20].

As result, this approach emphasizes the need of precise, segmented fabrication by LAO for SiNWT devices, with a particular emphasis on preserving nanowire gap homogeneity. This approach is consistent with previous advances in the fields and shows great potential for improving the accuracy and functionality of nanoscale electronic devices. This systematic methodology highlights the significance of segmented LAO manufacturing with AFM resting intervals, finally producing clear and well-defined SiNWT device design. These discoveries add to the continuing discussion about sophisticated nanofabrication methods. The micrograph pictures used in this work were taken at multiple periods, indicating varied dates and timestamps, because the fabrication process of segmented SiNWT structures needs lengthy attention and time to provide identifiable results characterized by cleanliness and accuracy.

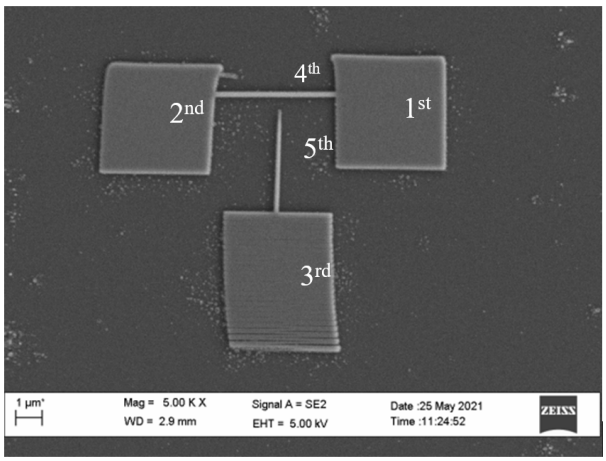
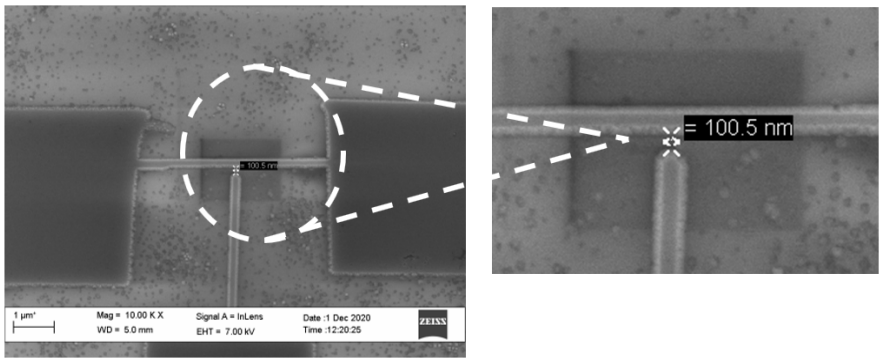
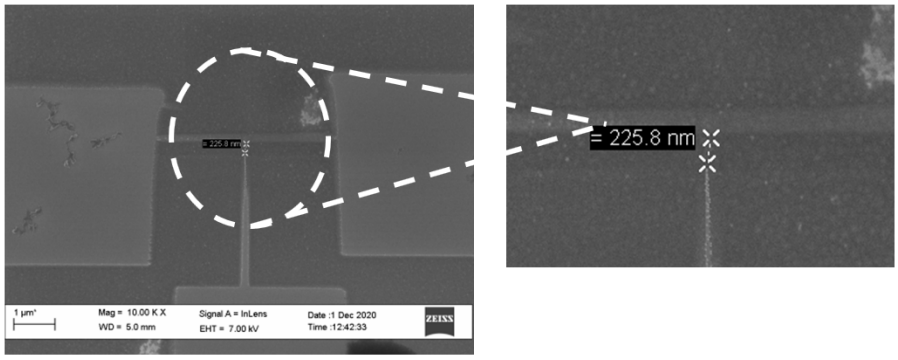


Fig. 5 *Final structure of the SiNWT was fabricated via LAO which developed partial by partial process (partial 1th–5th)*

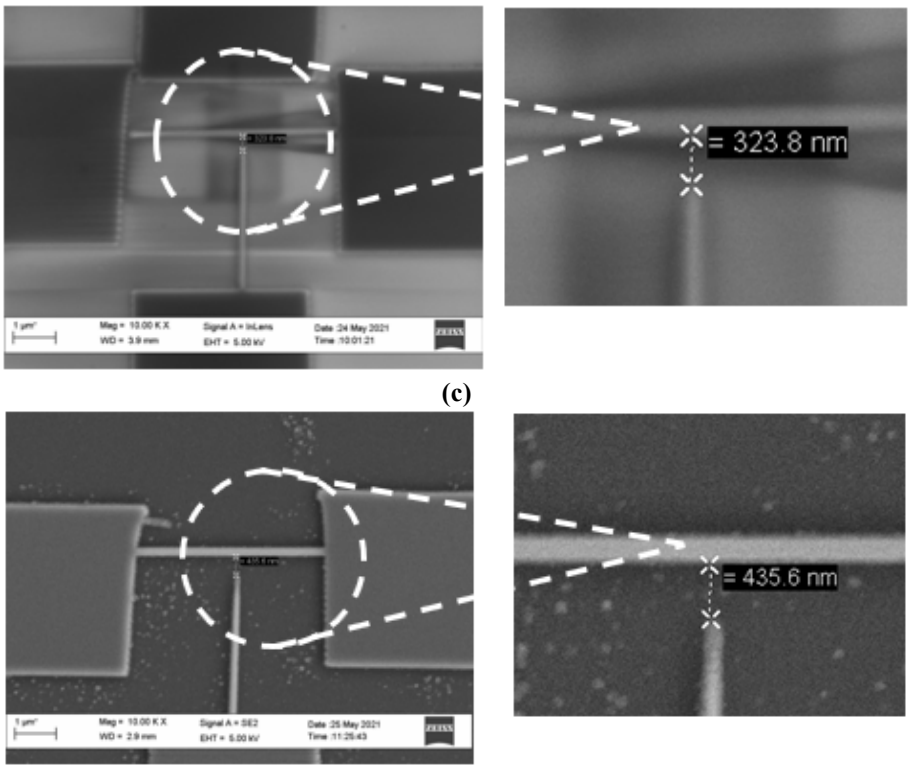


(a)



(b)

Fig. 6 *SiNWT structure with nanowire gap (a) ~ 100.5nm, (b) ~225.8nm*



(c)

(d)

Fig. 7 *SiNWT structure with nanowire gap (c) ~ 323.8nm, (b) ~435.6nm*

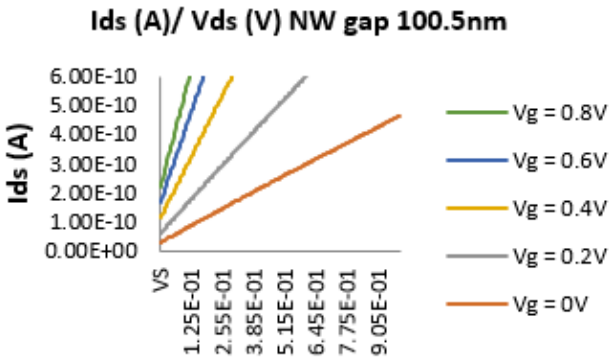
4.1 Effects on the I-V_{ds} Data on Variation of Nanowire Gap for SiNWT

An in-depth study of SiNWT structural changes for the purpose of electrical characterisation is presented in this paper. There utilised a Semiconductor Parameter Analyzer (SPA) coupled to the Desert Cryogenics HP4156 CSPA series software analysis model to aid this investigation. Applying bias voltage was required to characterise the electrical behaviour of SiNWs. Amazingly, at these low voltage levels, nanowires displayed linear ohmic behavior that was supported by empirical evidence and in accordance with the rules of Ohm's law, as described in Semiconductor devices: physics and technology (2nd edition) [21]. The importance of channel width and nanowire size as crucial factors controlling output characteristics is also emphasized in article [16]. These revelations served as the inspiration for this research, which adopted comparable ideas while investigating distinct manufacturing techniques. The Silicon-on-Insulator (SOI) substrate's doping concentration also significantly influenced the output values. Due to the samples' same substrate origin, it is remarkable that the experimental structure preserved a constant doping concentration across samples. Notably, different doping doses can have different outcomes, found that greater doping concentrations were linked to better electrical responses [1]. These collective findings highlight the complex electrical behavior of SiNWT, which is impacted by nanowire diameters, doping levels, and novel production techniques.

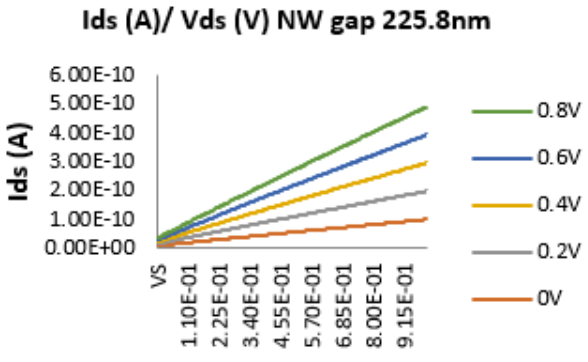
The fundamental concept claims that both contact resistance and external resistance can be regarded as insignificant in the context of resistant membrane nanowires. Additionally, as active crystalline silicon serves as the main component for the creation of SiNW, tremendous care is necessary during the nanofabrication process to maintain the layer's immaculate electrical characteristics. After fabrication, the SiNW serves as the fundamental building block of a Field-Effect Transistor (FET) structure when the gate electrode is added. Another vital aspect is the issue with extremely thin gate oxide layers, which is explained in Book Chapter [21]. Reduced gate capacitance and decreased trans conductance are the effects of excessive gate oxide thinning. Therefore, although not offering a perfect answer, improving the structural design by tackling miniaturization issues is crucial for optimizing device performance. The introduction of air gaps becomes an achievable option for reducing capacitance between the gate and channel when it is understood that a transistor's optimal performance is affected by a variety of parameters. Recent investigations [18-20] have confirmed that this decrease in parasitic fringe capacitance provided by the air gap also helps to lower sub-threshold slopes, providing considerable power savings during switching operations when applied to the transistor. These findings, which reflect the current state-of-the-art in nanoelectronics, highlight the complicated interplay between design considerations and fabrication processes in optimizing transistor performance.

In the case of the recently fabricated SiNWT devices, the predominant operational mechanism is the dissolution of chemical bonds inside the channel area or the creation of new electronic states, principally brought on by changes in gate voltage. The amount of charge that may become trapped inside the Buried Oxide (BOX) layer and the channel is regarded as insignificant within the device construction. Therefore, bond-breaking events are the main cause of threshold voltage alterations. This behavior, as described in the cited article [19], is inextricably tied to the gate voltage and manifests as a crucial element influencing the change from the device's 'on' to 'off' states. As a result, the significant decrease in trans conductance illustrates how a positive gate voltage causes channel depletion. These experiments include a variety of input voltages to thoroughly examine this feature, illuminating the relationships and impacts of the nanowire gap or air gap on the final output voltage.

Fig. 7 (a), (b), (c), and (d) demonstrate the output characteristics of the SiNWT at various positive gate voltages, and they offer important insights. In accordance with information from earlier investigations, current-voltage (I-Vds) characteristics were measured in the 0-0.6 V input voltage range while accounting for a device off-state leakage of around 0.8 V. The findings show a recurrent and notable pattern of nanowire gap broadening, which is compatible with the findings of the cited publications [3,20,22]. These results support the assumption that carrier behavior is significantly influenced by gate proximity to the channel. Smaller gap devices experience an off-current drop of three orders of magnitude while relying on electrostatic carrier management for on-state current. Particularly in solid insulators, the addition of nanoscale air gaps efficiently reduces leakage currents via the gate and channel. Additionally, when positive voltage rises, the linear output gate voltage pattern denotes a change to accumulation mode. However, additional current augmentation is only marginally effective at high gate voltages. As gate voltage increases, the strong electric field's impact on the channel causes a considerable number of carriers from Regions I and III to be directed towards Region II, causing the phenomenon to occur [3,18-20,22].



(a)



(b)

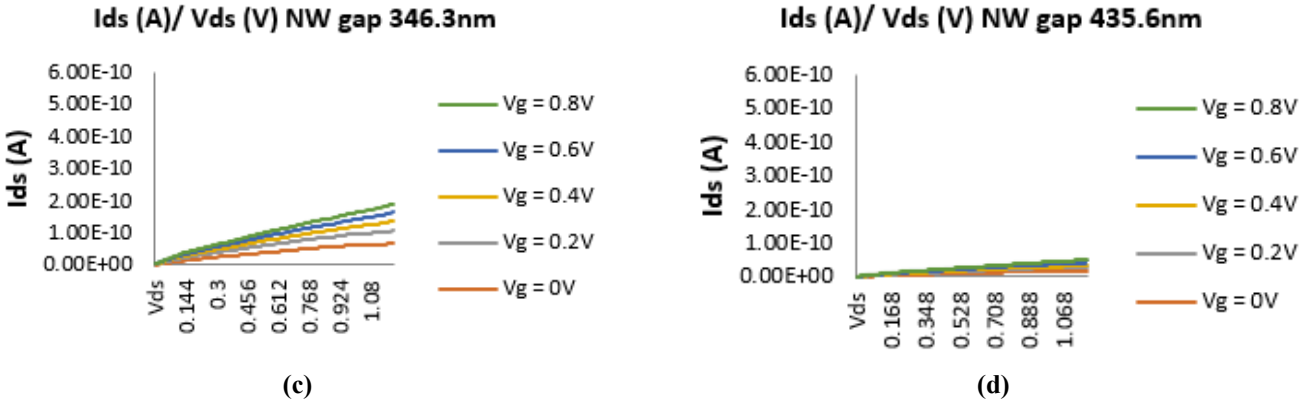


Fig. 7 *Output voltages of the I-V characteristics at low voltages (0-0.8V) for varies nanowire gap (a) Nanowire gap 100.5nm, (b) Nanowire gap 225.8nm, (c) Nanowire gap 346.3nm, (d) Nanowire gap 435.6nm*

5. Conclusion

In the current experimental study, the research concentrates on examining the I_{DS}-V_{DS} properties of nanowires at low voltages, namely in the region of 0.2-0.8 Volts, while systematically altering the nanowire gap. The reason of input voltage at maximum 0.8V is because more than that value, the device tends to breakdown. The main goal is to determine how output voltages are impacted by nanowire gap diameters. Notably, the device changes into accumulation mode as the applied positive gate voltage rises. However, even at higher gate voltage inputs, the effect of the electric field on the channel at low gate voltages is still negligible, leading to a negligible change in current. The significance of the electric field's intensity in affecting channel behavior is highlighted by these phenomena. Significantly, the changes in air gap and nanowire gap diameters that have been found strongly demonstrate this claim the output voltages are significantly impacted by these variations, further demonstrating the relationship between electrical properties and nanowire gap diameters. These results support previous research, such as the work of Wang, J., & Xu, M. in 2023, which emphasizes the value of nanowire gap engineering in the development of nanoelectronic devices [3]. Similar to our findings, the work of Zhang, Q et. al in 2022 clarifies the crucial function of gate voltage in modifying device behavior [20]. In conclusion, the results from this study in general can be concluded, as the nanowire gap increases, the current (I) tends to decrease, especially in the on-state of the transistor. This is because a wider gap can lead to reduced carrier mobility and increased resistance within the channel, making it harder for current to flow. It will give extensive evidence for the relationship between output voltages and nanowire gap diameters, particularly in the setting of low voltage regimes. Future nanoelectronic design approaches may be influenced by this information, which adds delicately to the current understanding of nanowire-based device performance.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of the paper.

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